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MS-7358 uATX **Version: 3.0**

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35 North Bridge
Intel ICH9 (DO South Bridge)

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635
LAN -- INTEL NINEVEH/EKRON
HD Audio Codec -- ALC883
1394 Controller -- VT6308 (2-port)
PCIE to PATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

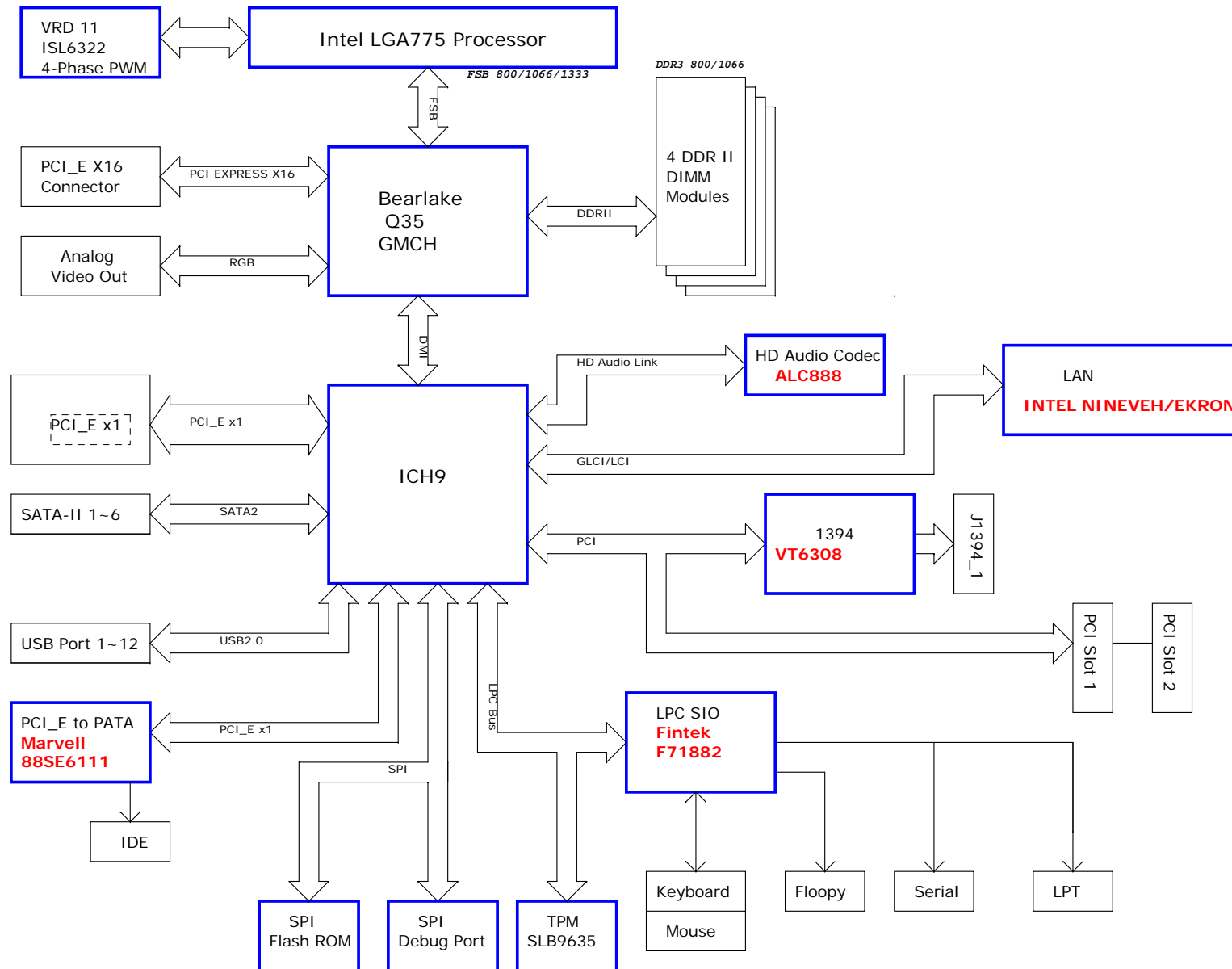
Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-Q35/ICH9DO	cfg-7358-STD	



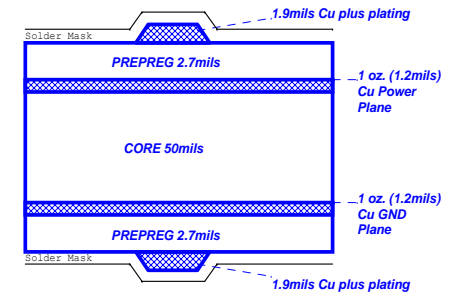
MICRO-STAR INT'L CO.,LTD			
MS-7358			
Size Custom	Document Description COVER SHEET	Rev 3.0	
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Block Diagram



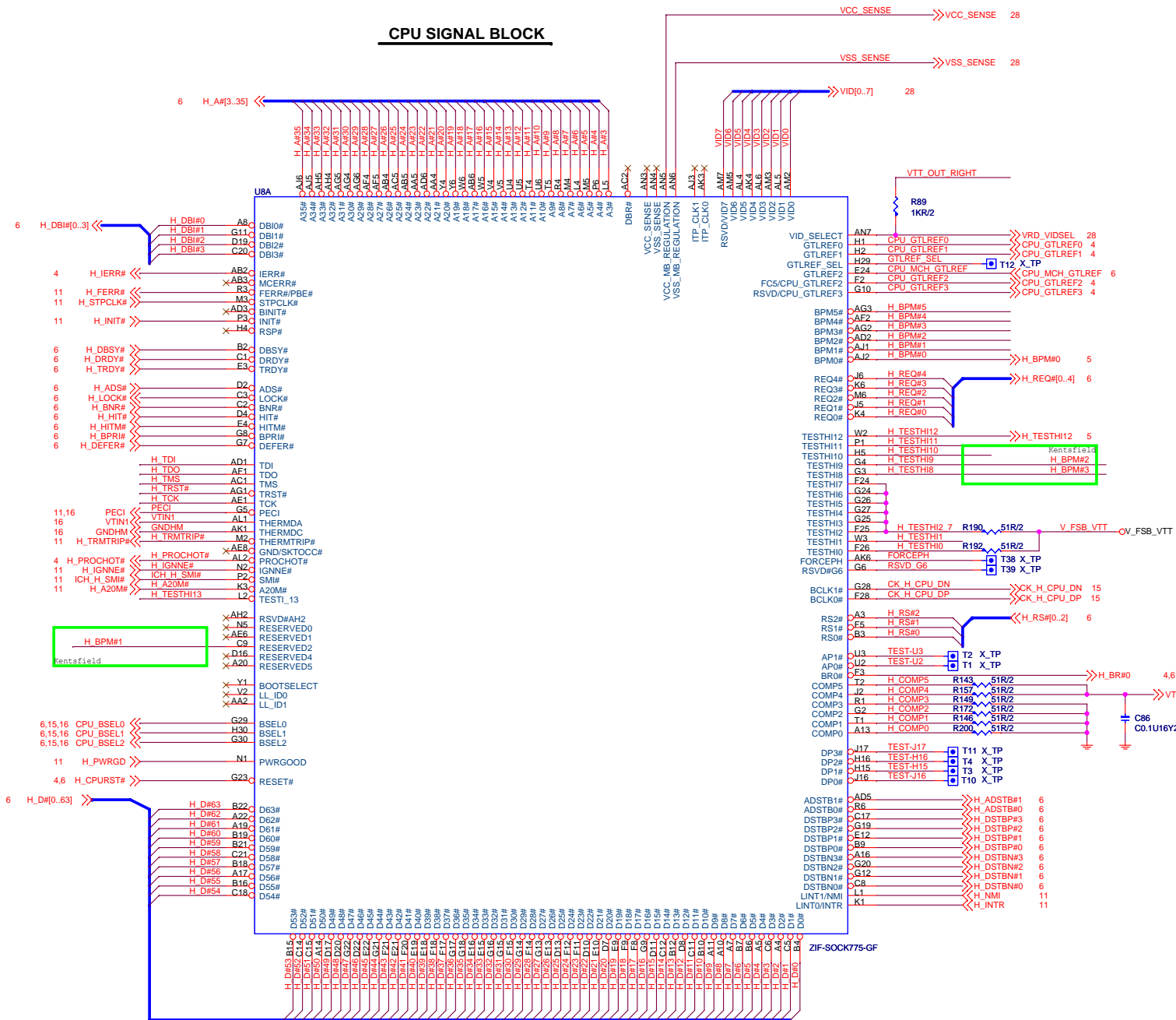
Board Stack-up

(1080 Prepreg Considerations)

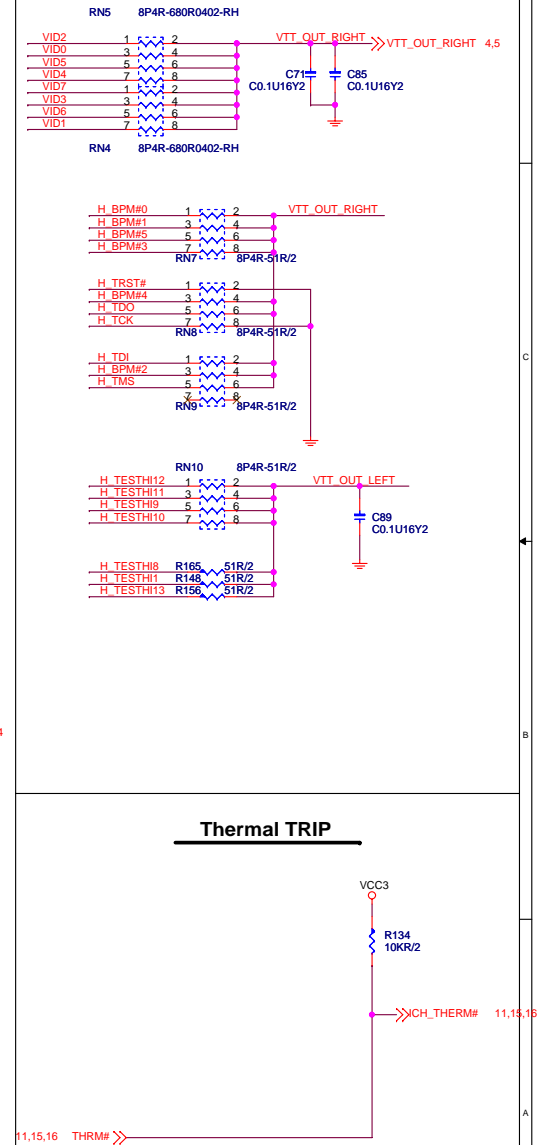


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

CPU SIGNAL BLOCK



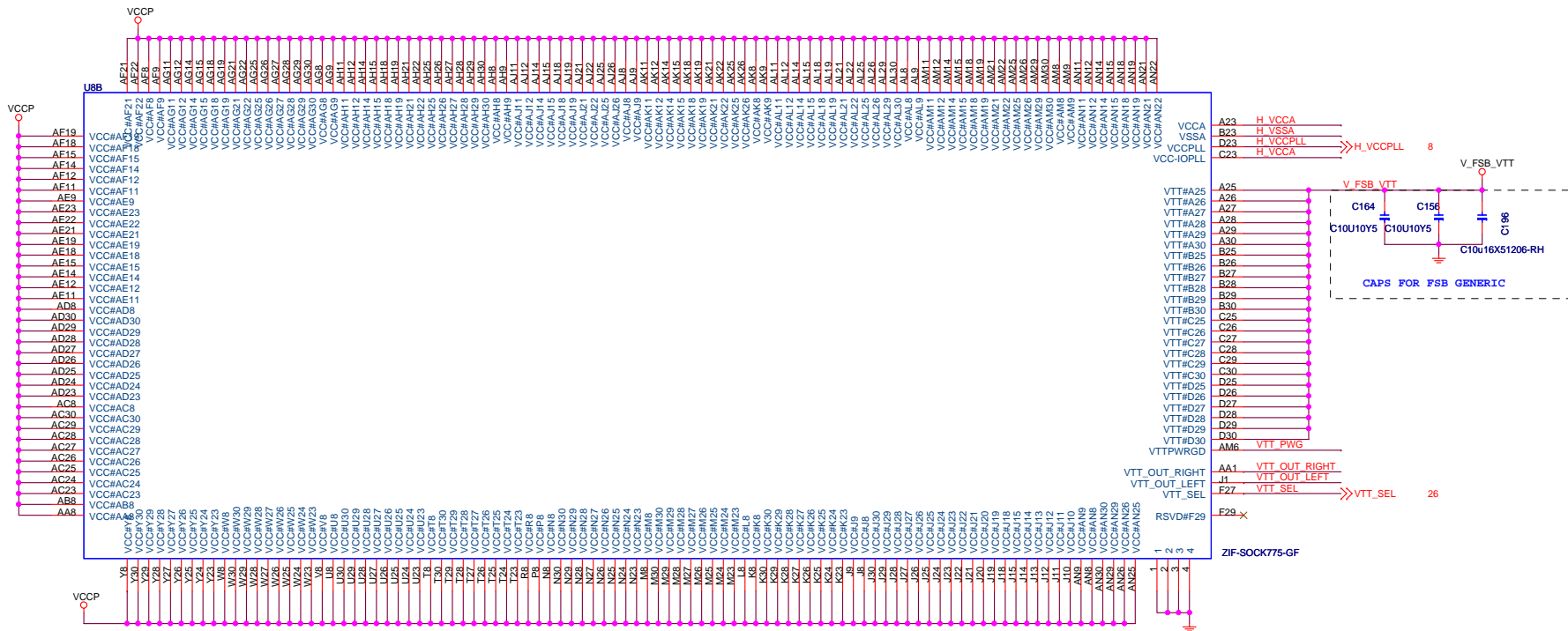
PULL HIGHT PULL DOWN



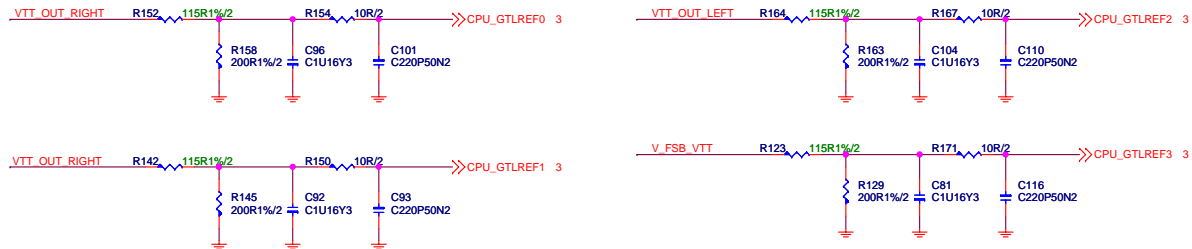
MICRO-STAR INT'L CO.,LTD

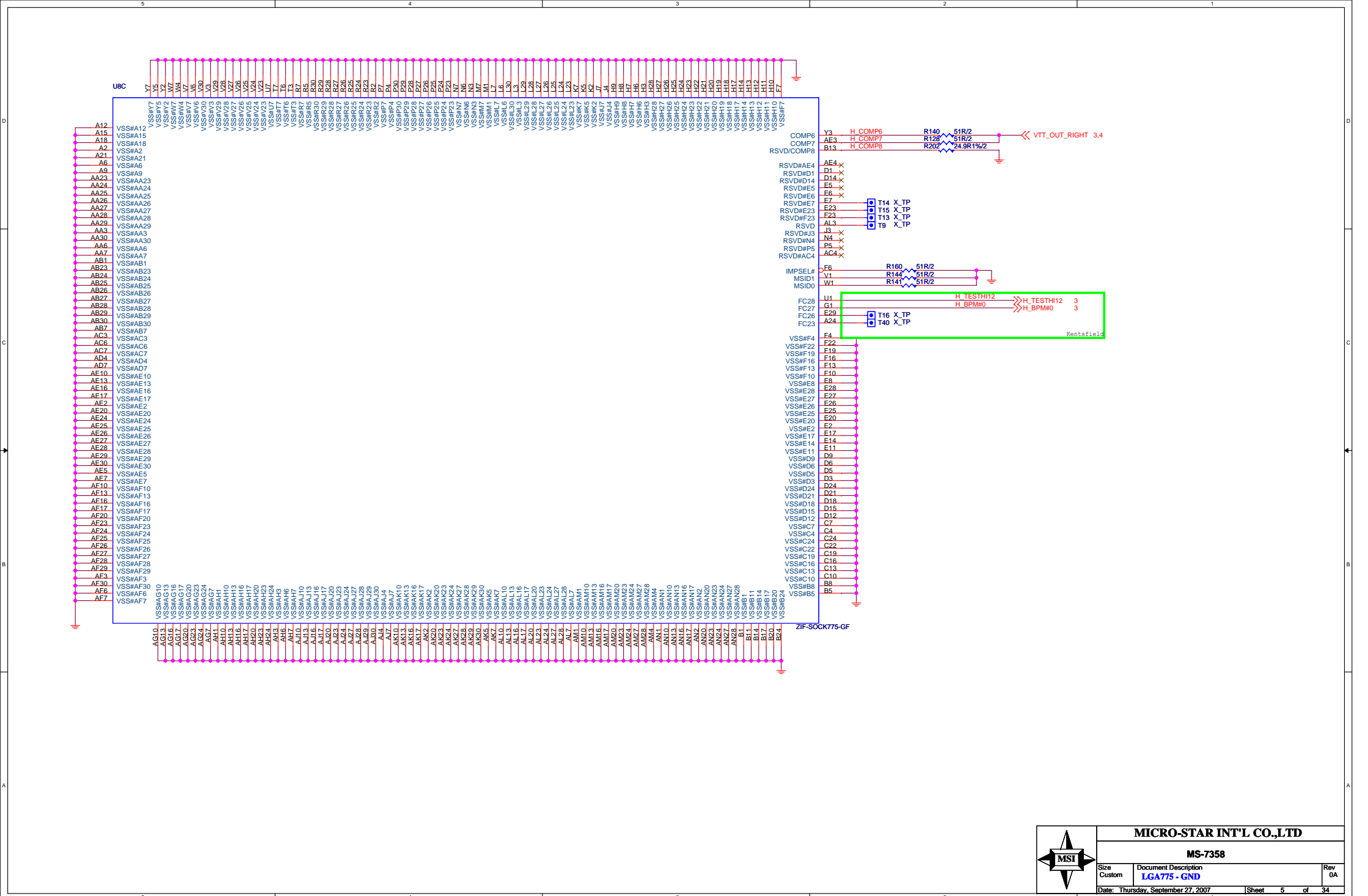
MS-7358

Size Custom	Document Description LGA775 - Signal	Rev 0A
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*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)

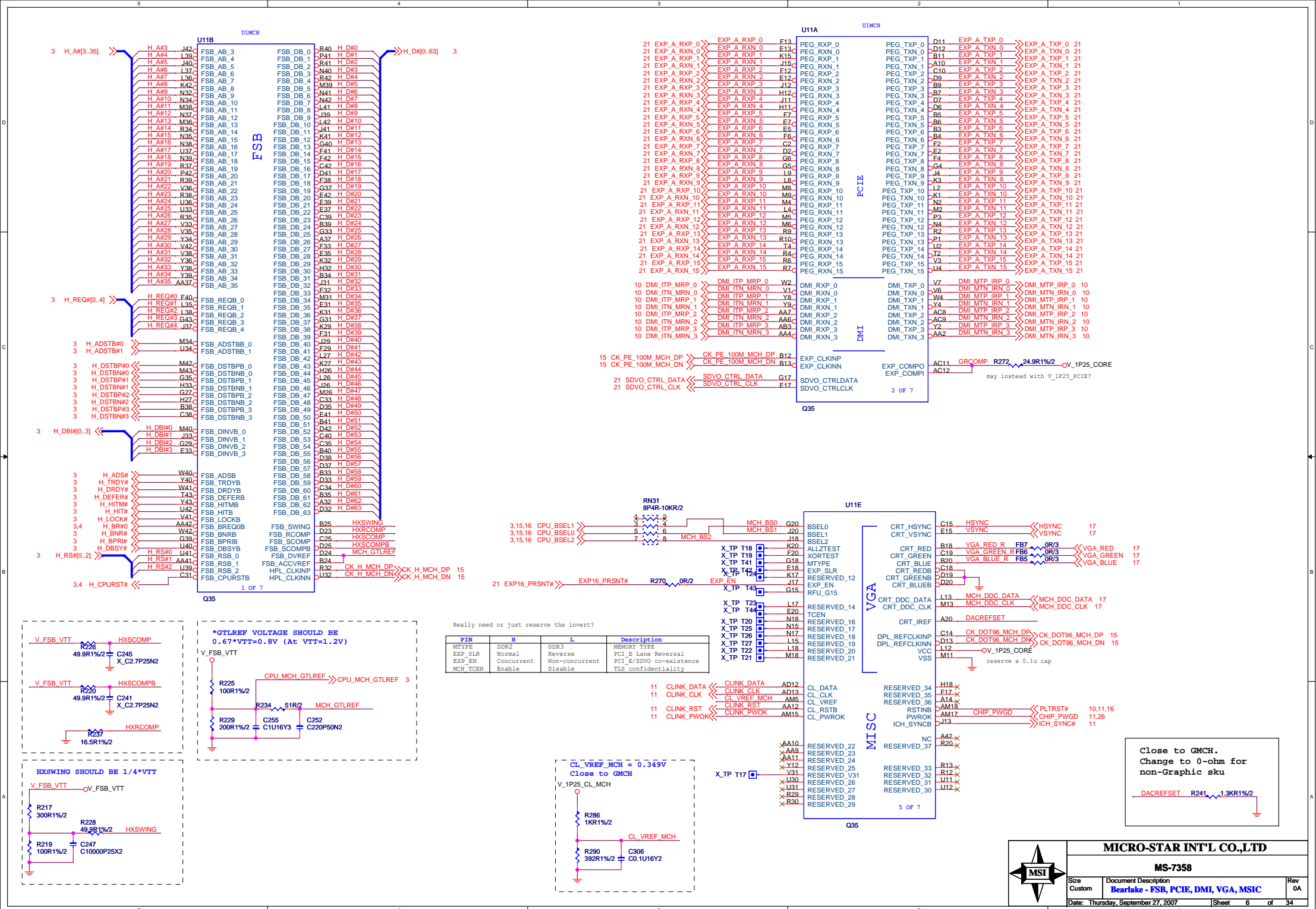




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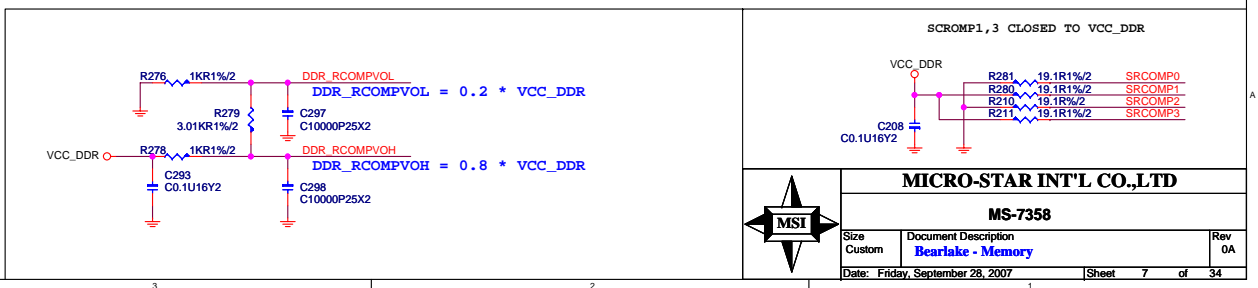
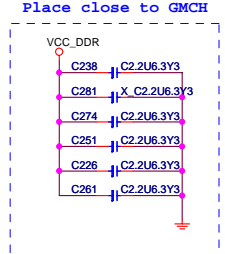
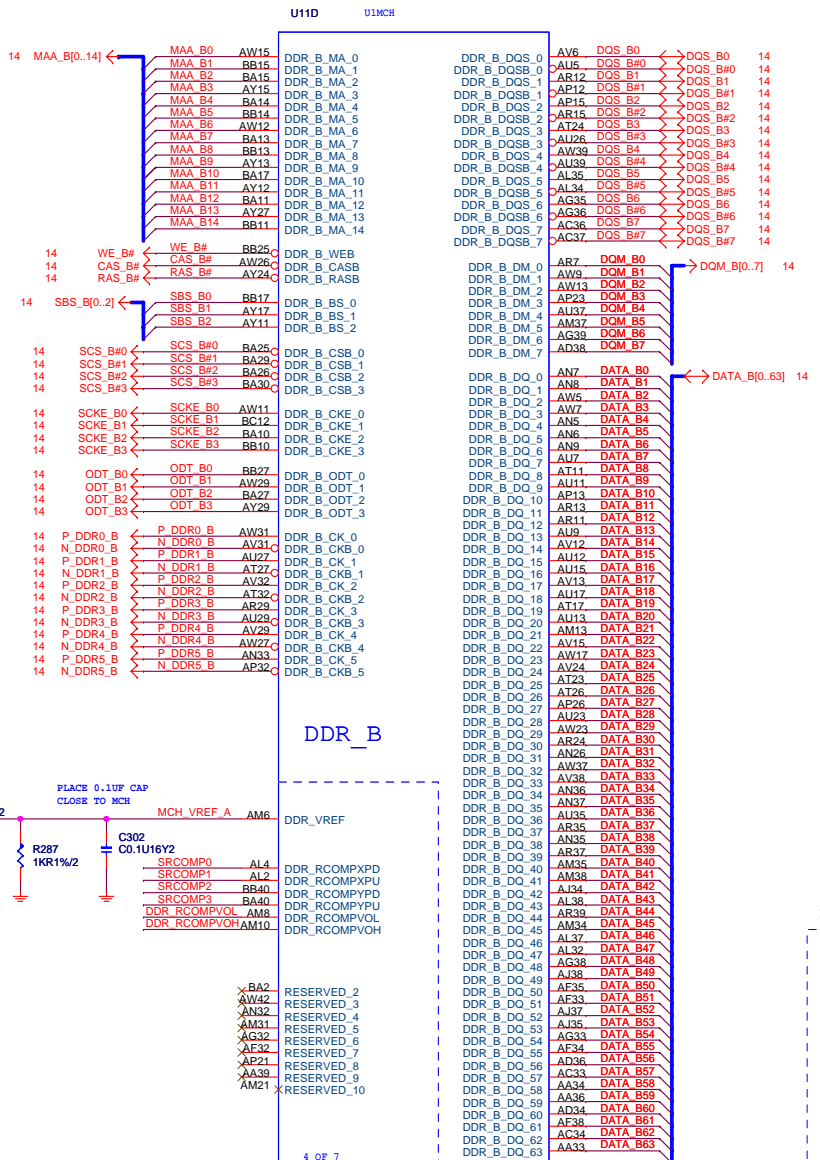
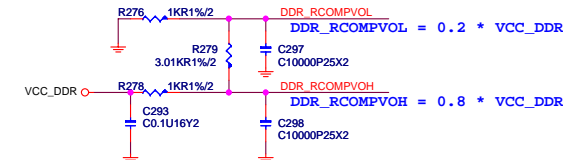
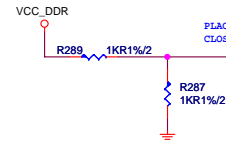
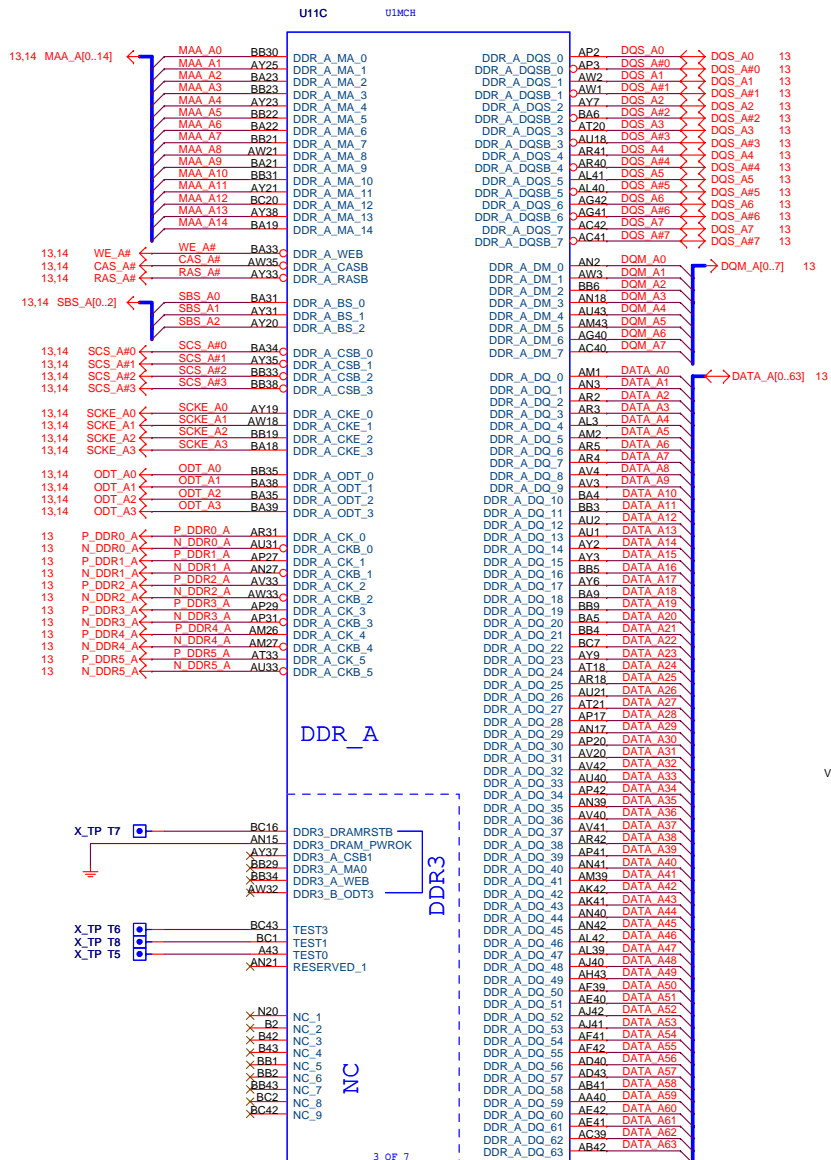
Size Custom	Document Description LGA775 - GND	Rev 0A
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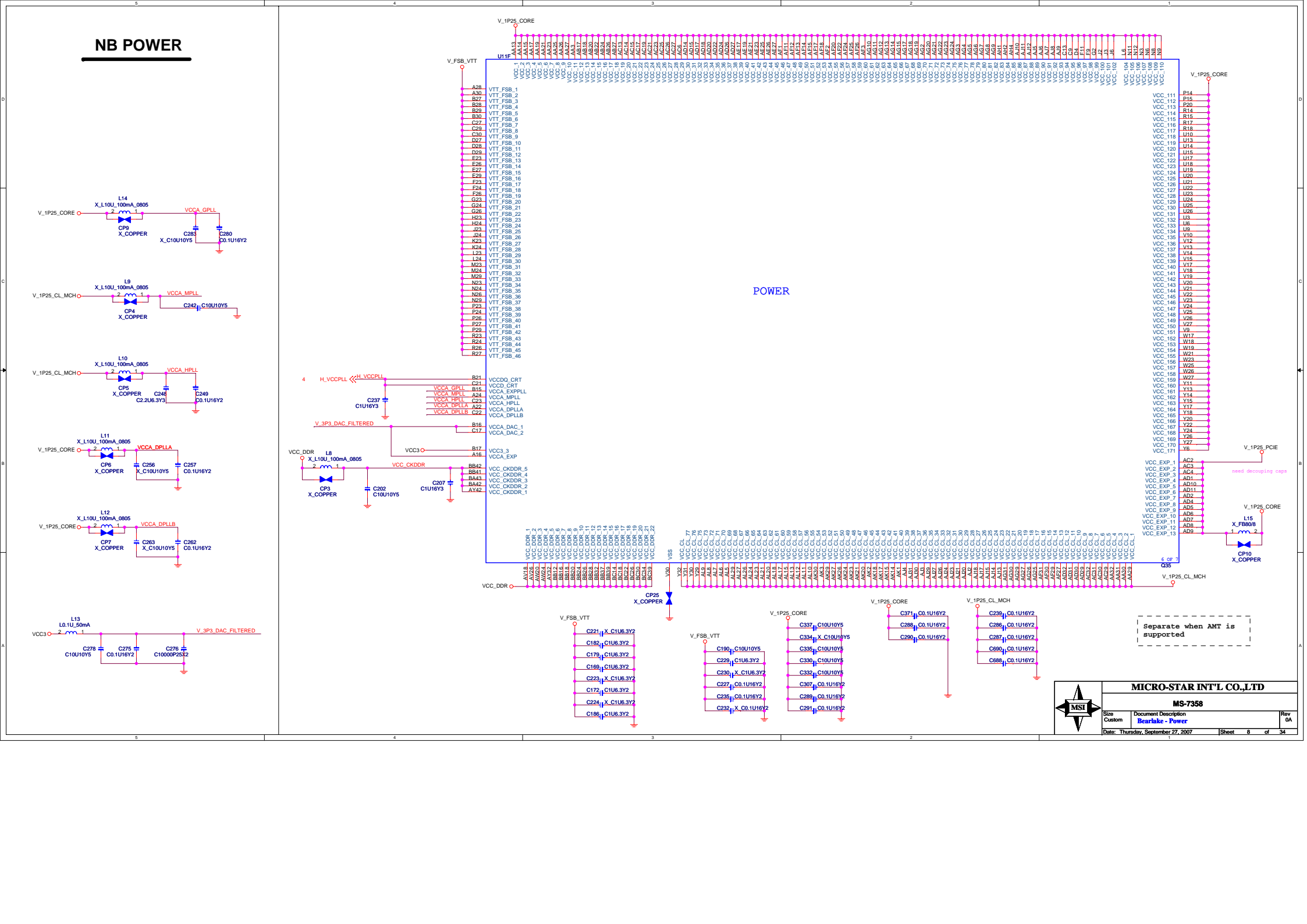
Size Custom	Document Description Bearlake - FSB, PCIE, DMI, VGA, MSIC	Rev 0A
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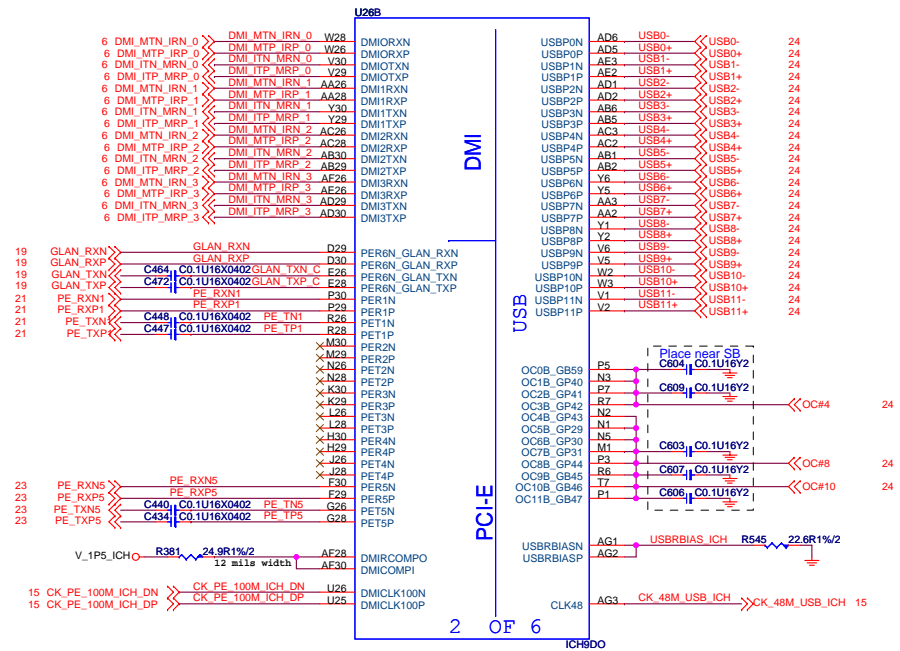
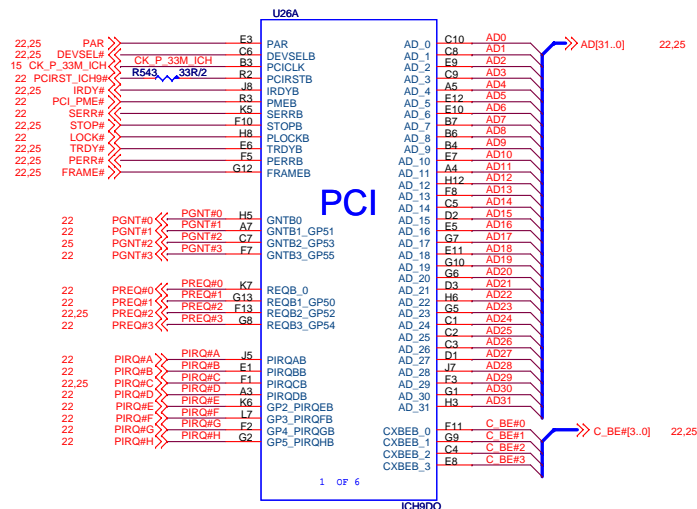


The image displays a detailed PCB layout for a power management system, specifically for a notebook (NB) power. The layout is organized into several functional areas:

- Top Left: NB POWER** - This section contains the main power input and distribution network. It includes a 10.1uH, 50mA inductor (L13) and a 0.1uF, 16V capacitor (C278) connected to the VCC3 pin. The output is connected to the V_3P3_DAC_FILTERED pin.
- Top Right: V_1P25_CORE** - This section shows the core power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L14) and a 0.1uF, 16V capacitor (C280) connected to the V_1P25_CORE pin. The output is connected to the V_1P25_CORE pin.
- Bottom Left: V_1P25_CL_MCH** - This section shows the memory and chassis power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L9) and a 0.1uF, 16V capacitor (C242) connected to the V_1P25_CL_MCH pin. The output is connected to the V_1P25_CL_MCH pin.
- Bottom Right: V_1P25_CORE** - This section shows the core power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L10) and a 0.1uF, 16V capacitor (C249) connected to the V_1P25_CORE pin. The output is connected to the V_1P25_CORE pin.
- Center: POWER** - This section shows the main power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L11) and a 0.1uF, 16V capacitor (C256) connected to the V_1P25_CORE pin. The output is connected to the V_1P25_CORE pin.
- Bottom Center: V_1P25_CORE** - This section shows the core power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L12) and a 0.1uF, 16V capacitor (C263) connected to the V_1P25_CORE pin. The output is connected to the V_1P25_CORE pin.
- Bottom Right: V_1P25_CORE** - This section shows the core power distribution network. It includes a 10.1uH, 100mA, 0.805 inductor (L13) and a 0.1uF, 16V capacitor (C278) connected to the V_1P25_CORE pin. The output is connected to the V_1P25_CORE pin.

The layout also includes various other components and connections, such as the V_1P25_CORE, V_1P25_CL_MCH, V_1P25_CORE, and V_1P25_CORE pins, and the V_1P25_CORE, V_1P25_CL_MCH, V_1P25_CORE, and V_1P25_CORE pins.

[illegible][illegible]



SB STRAPPING RESISTOR

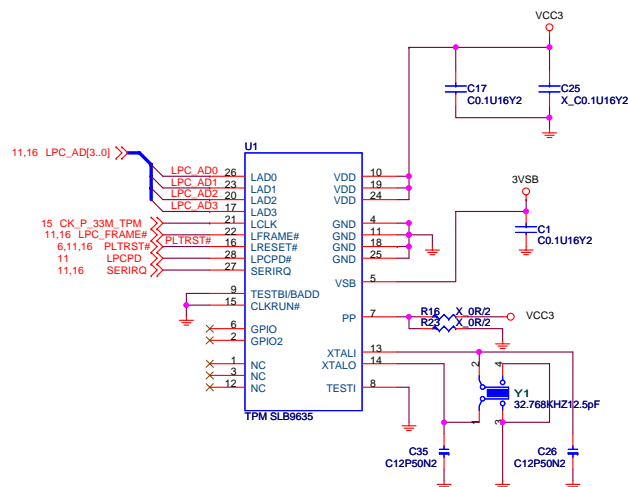
R539 1KR1%2 PGNT#0

BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCI PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0]. Internal weak pull down.
00:1X/1X/1X 11:0X/0X/4X

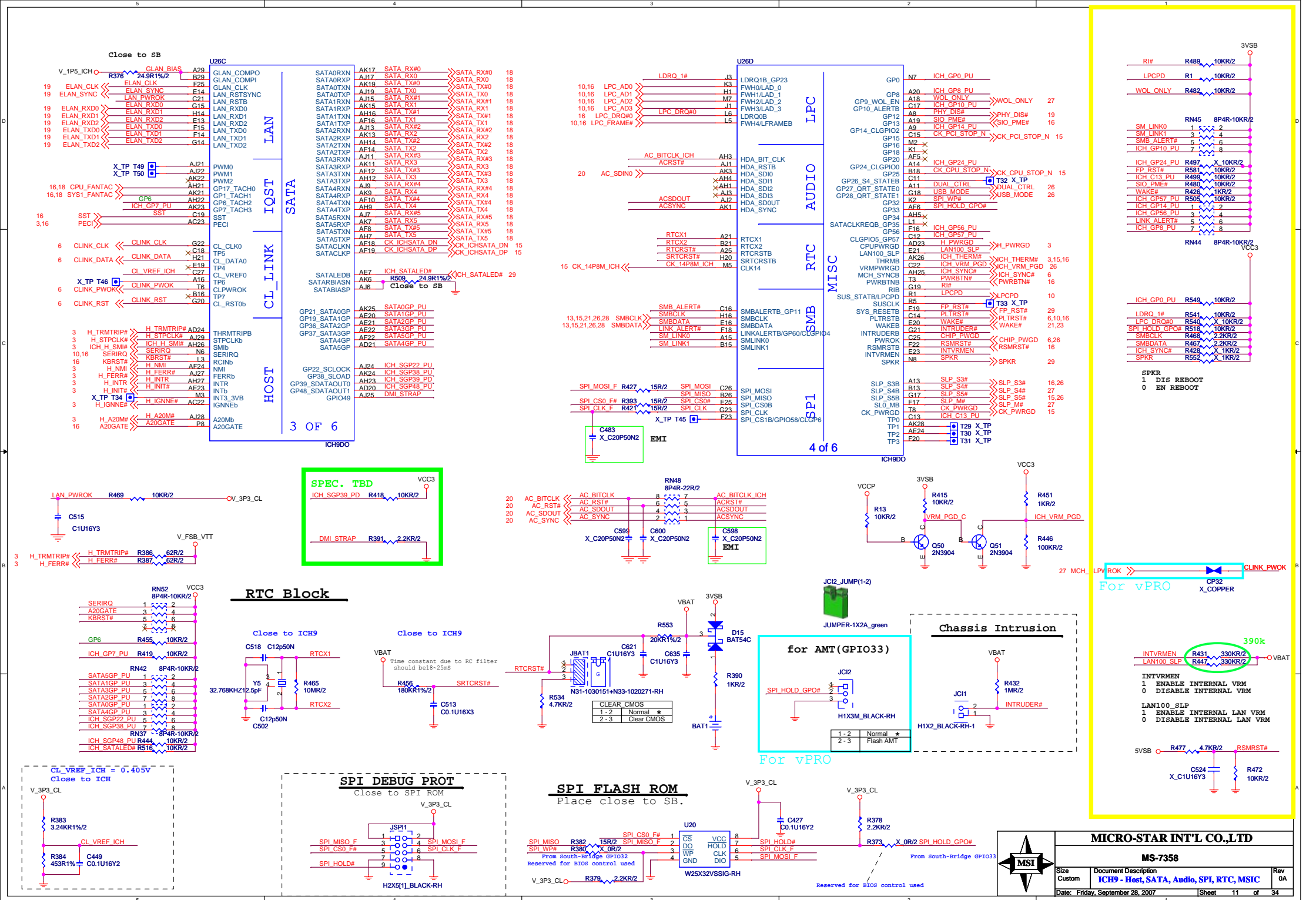
TPM - Security Controller



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Size	Document Description	Rev
Custom	ICH9 - PCI, DMI, USB, PCIe & Slots	0A
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V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



Size Custom	Document Description ICH9 - Power, GND	Rev 0A
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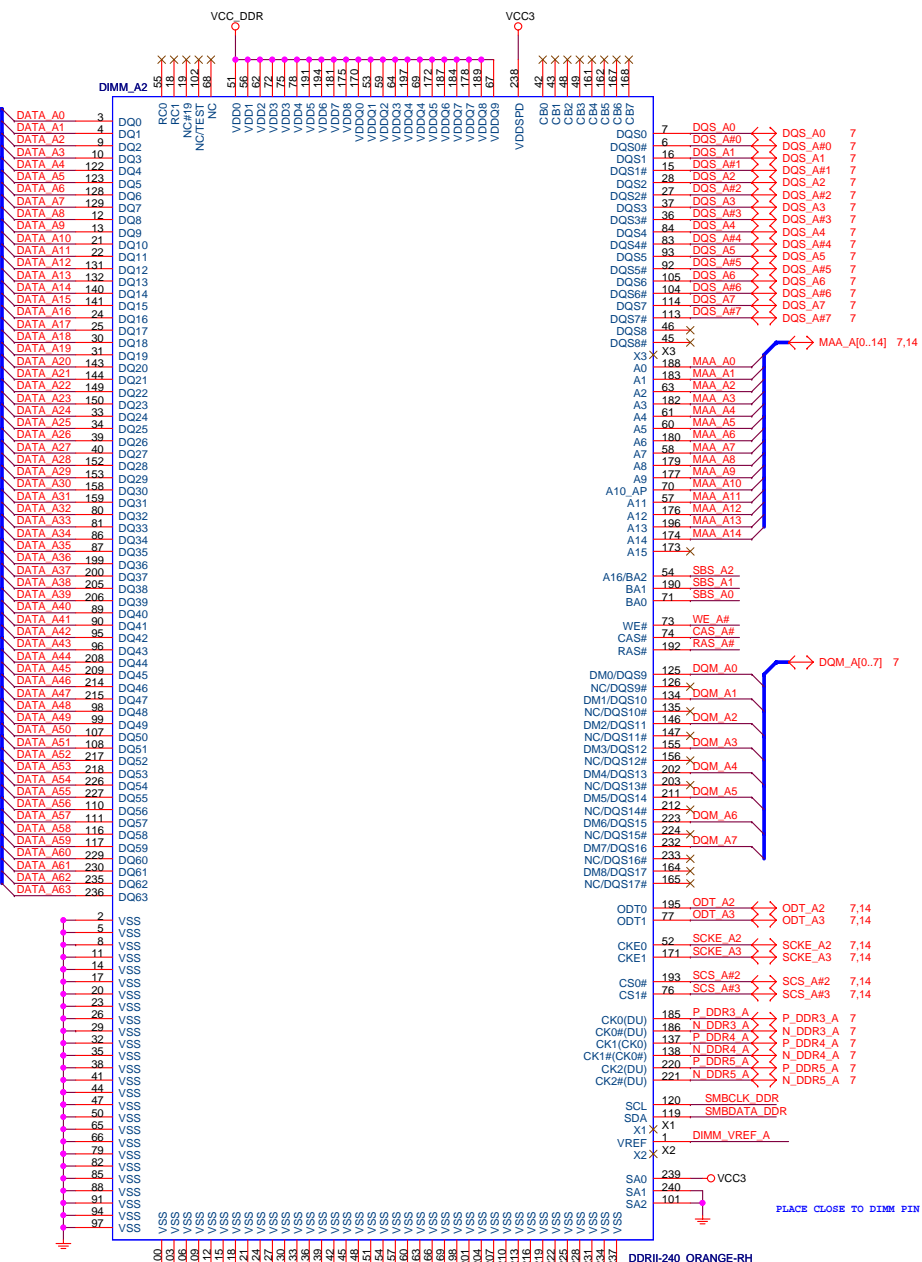
DDRII DIMM_A1



ADDRESS: 000
0xA0

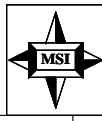
SMBCLK_DDR R76 33R/2
SMBDATA_DDR R80 33R/2

DDRII DIMM_A2

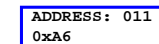
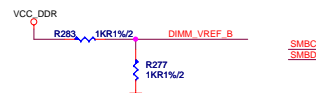
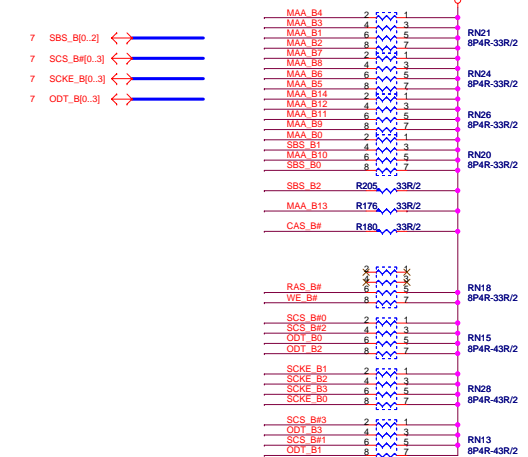


ADDRESS: 001
0xA2

SMBCLK_DDR R76 33R/2
SMBDATA_DDR R80 33R/2



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MS-7358		
Size	Document Description	Rev
Custom	DDR2 CHANNEL-A	0A
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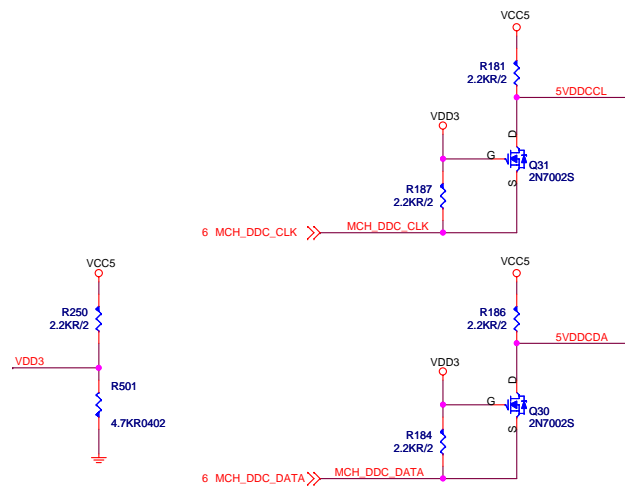
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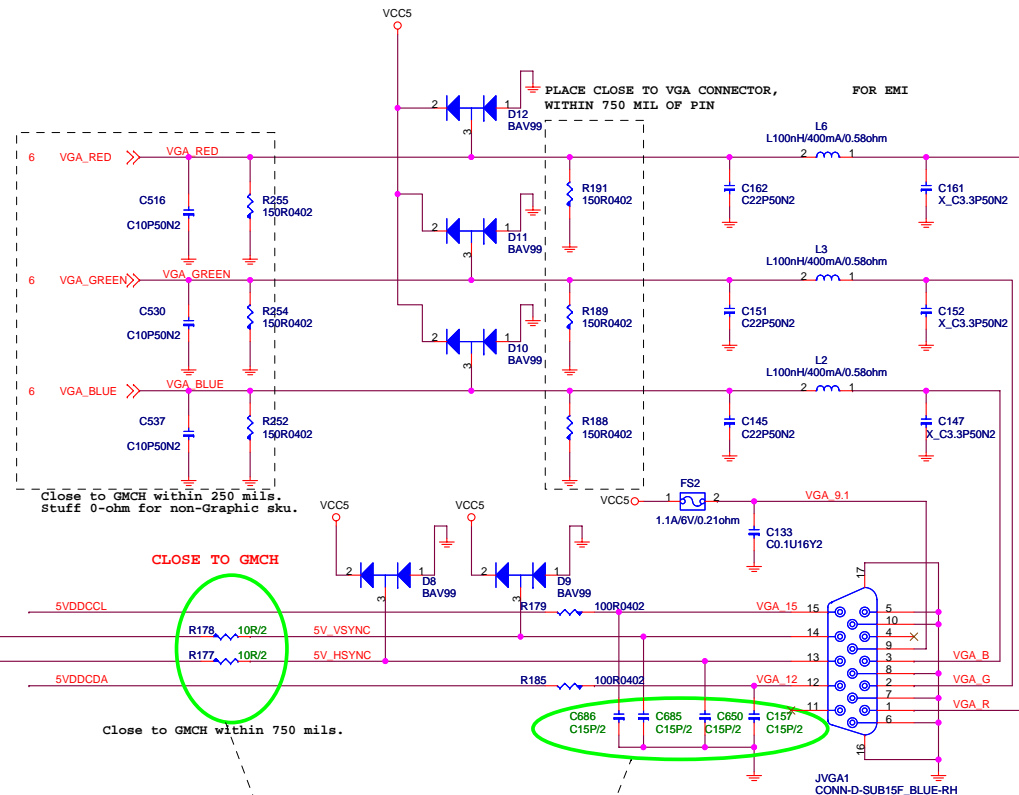
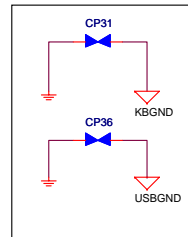
MS-7358

Size Custom	Document Description DDR2 CHANNEL-B/DDR II Termination
Date: Thursday, September 27, 2007	Sheet 14 of

Video Connector



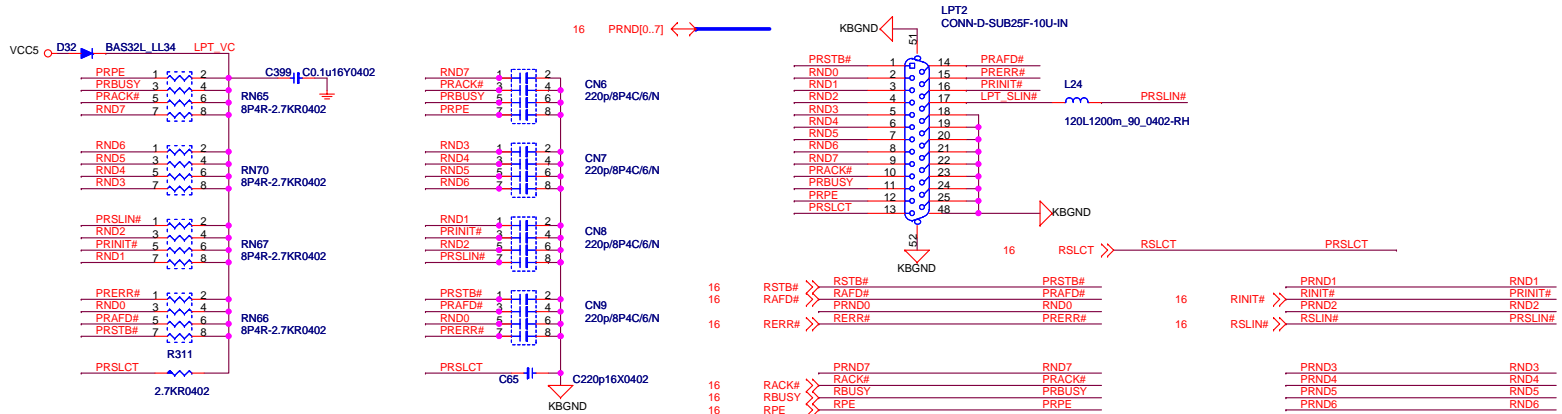
EMI SOLUTION



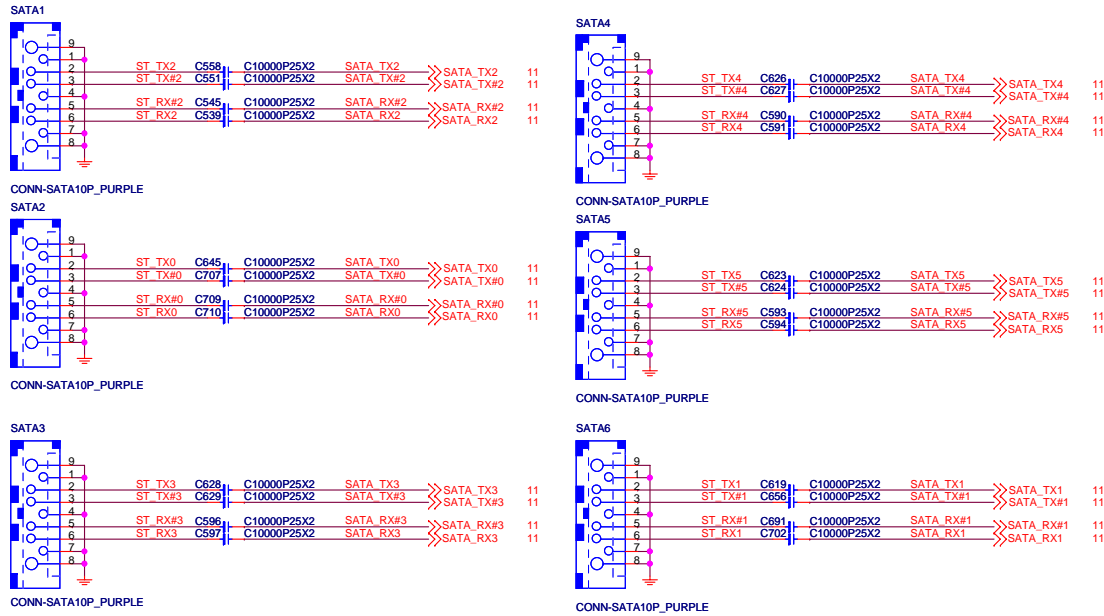
Close to GMCH within 750 mils.

Modify HSYNC/VSYNC Circuit
1. R178, R177 from 30R to 10R
2. CN3 from 33p to 15p
For Rise time edge not clean 07.3.30 by Robile

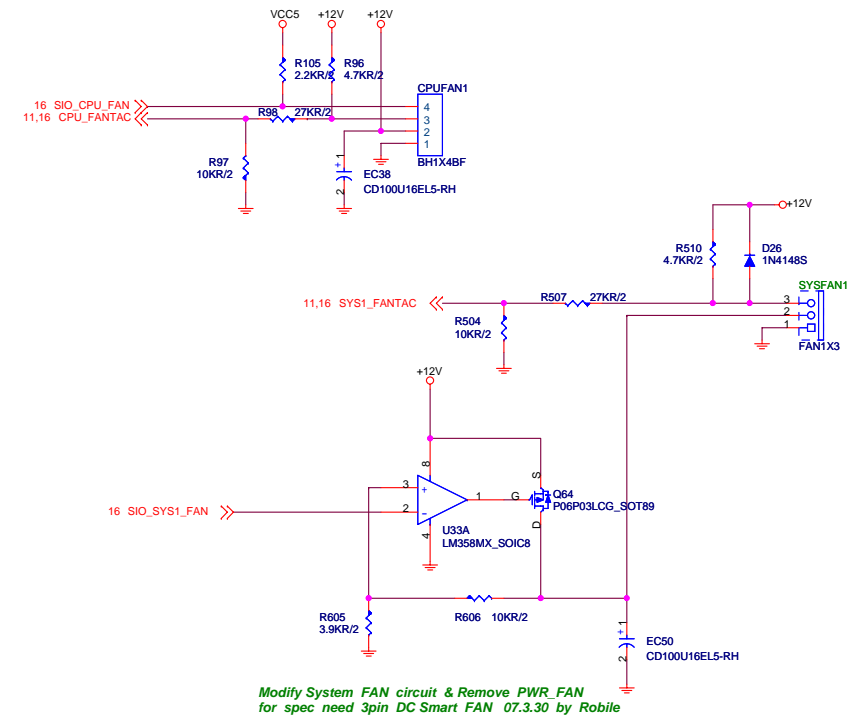
PARALLAL PORT



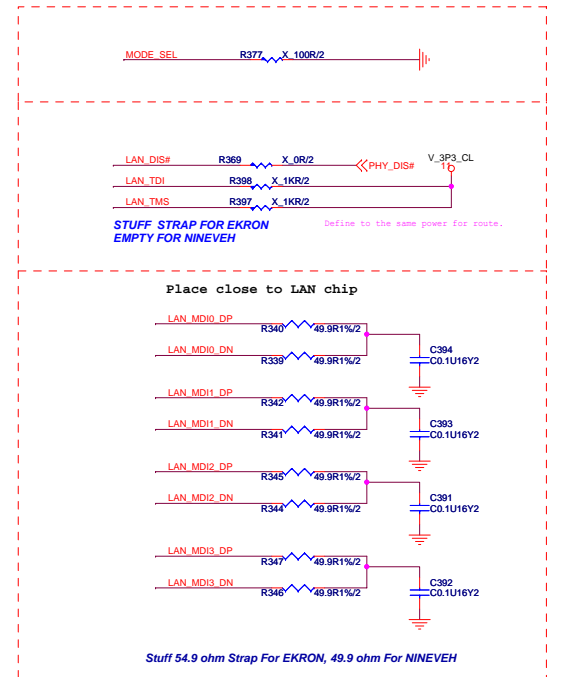
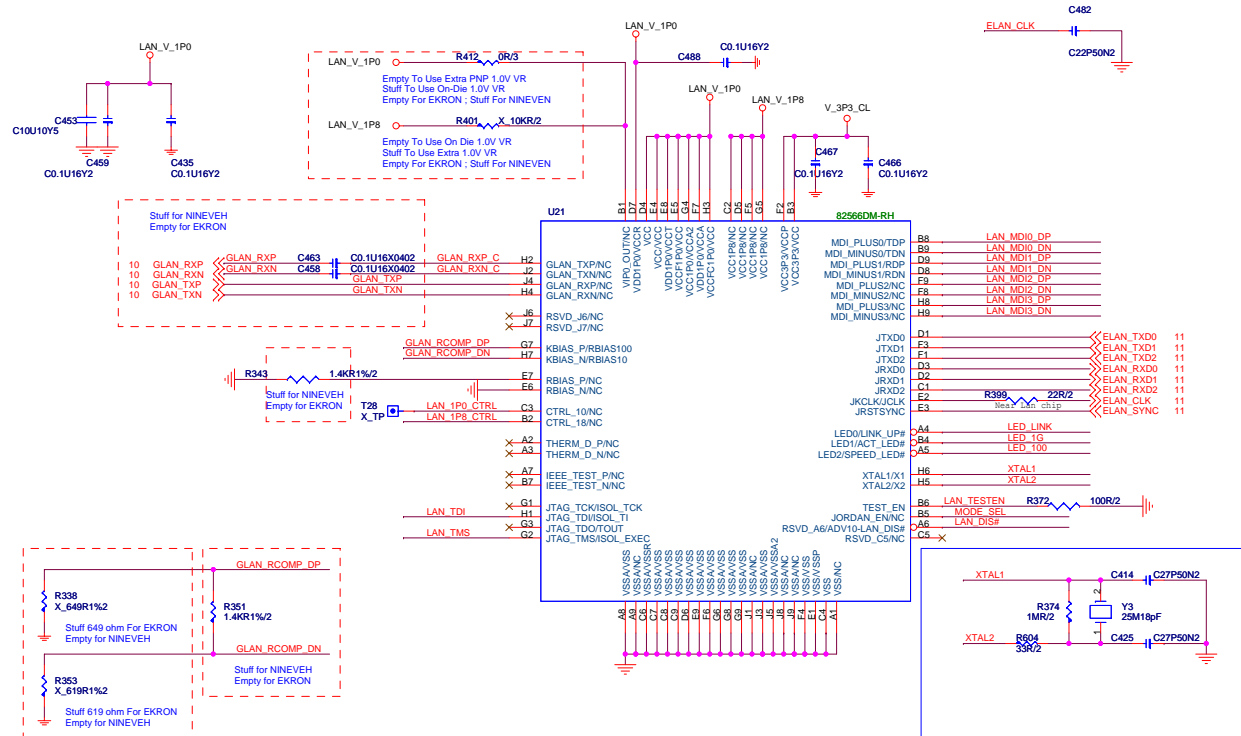
SATA 1- 6 PORT



FAN-COUNTROL CIRCUIT



LAN - NINEVEH/EKRON



Intel 82566DM
For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multipoint teaming,RSS,Intel Stable Image Platform Program drivers.
Intel 82566DC
For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
Basic 10/100 Ethernet connection.
B06-8256605-1Y6
FOR NECP CONSIGN,CHIP LAN,INTEL/82566DM,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE
B06-8256615-106
,CHIP LAN,INTEL/82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE
B06-8256205-106
,CHIP LAN,INTEL/82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

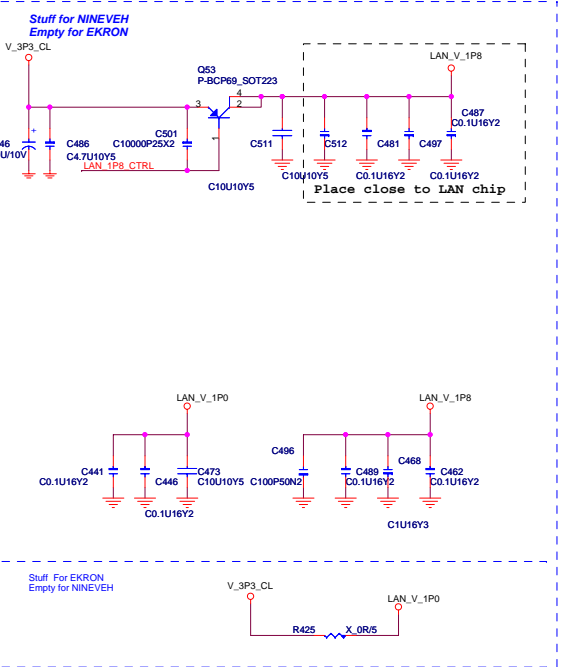
Modify Lan CLK circuit only BOM changes 07.3.30 by Robile

Speed LED Type
1000Mbps : Orange
100Mbps : Green
10Mbps : LED off

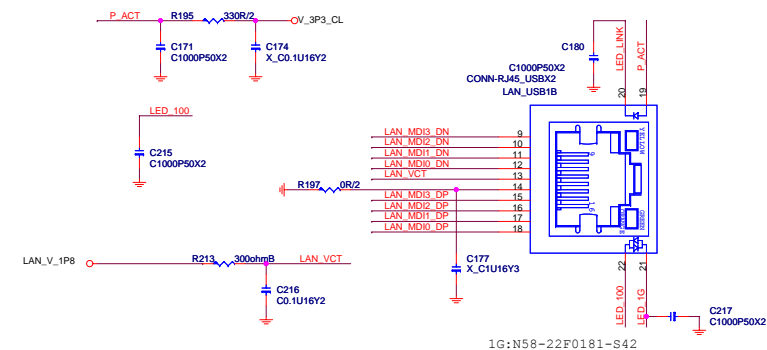
YELLOW : For Active/Link

ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN--LOW WOL DIS--HIGH

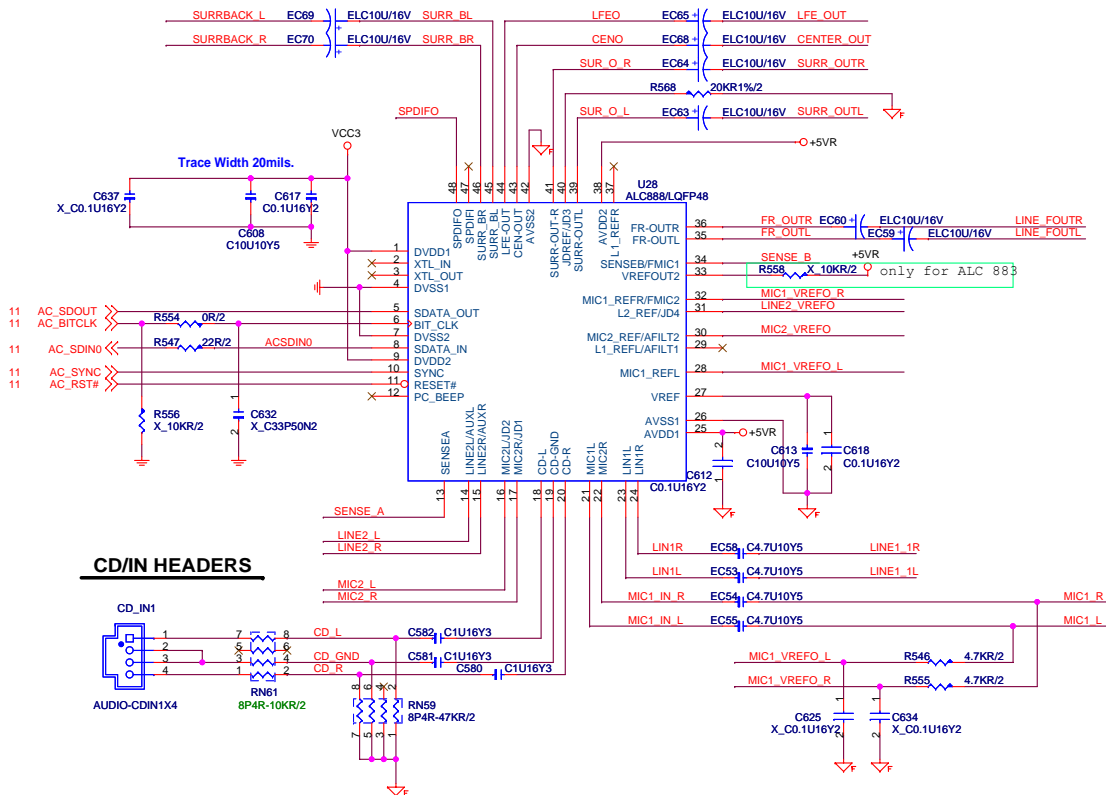
Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0061-P02
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	10 None
19	19
20	20
21	21
22	22



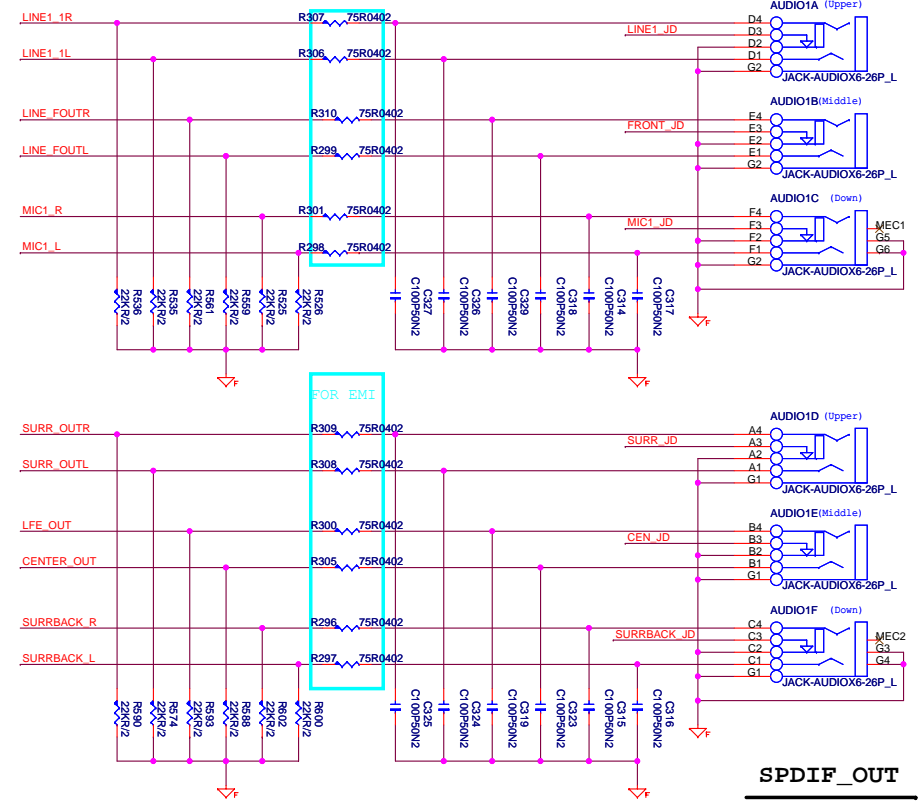
LAN CONNECTOR



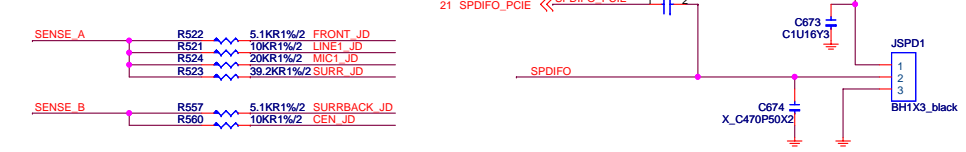
ALC883 CODEC



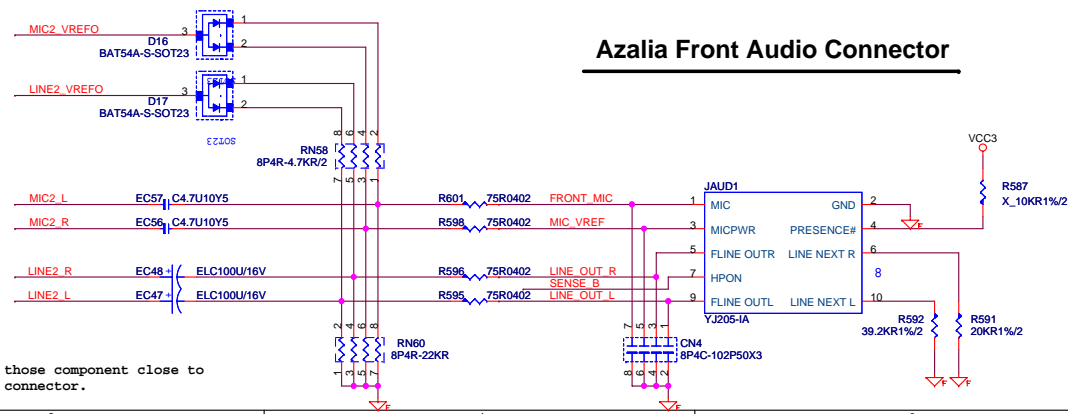
ALC883 JACK



ALC883 JACK DETECT

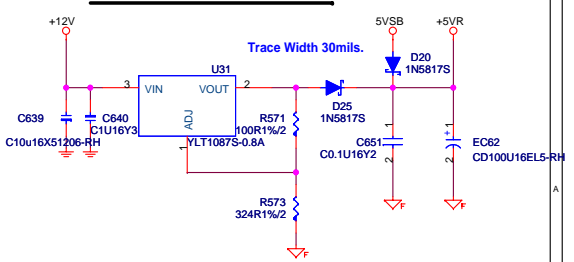


Azalia Front Audio Connector



Place those component close to audio connector.

AUDIO CODE REGULATORS

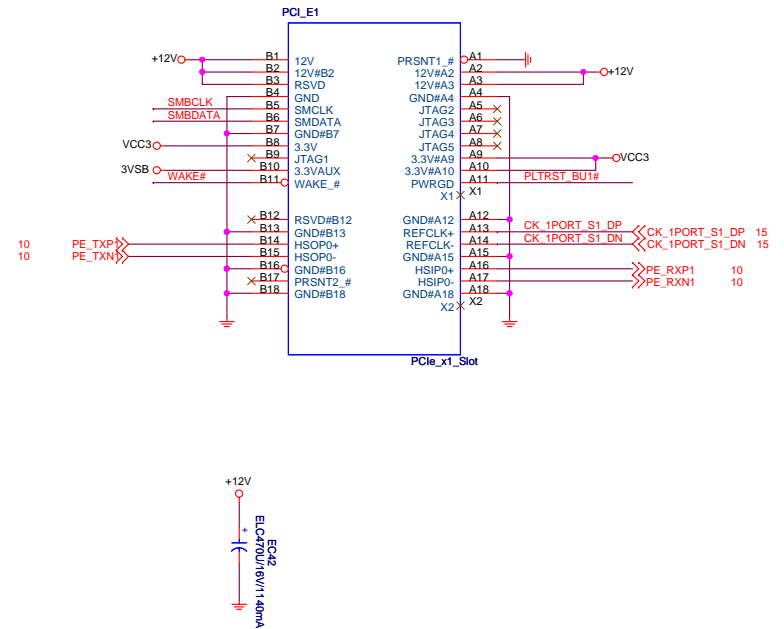


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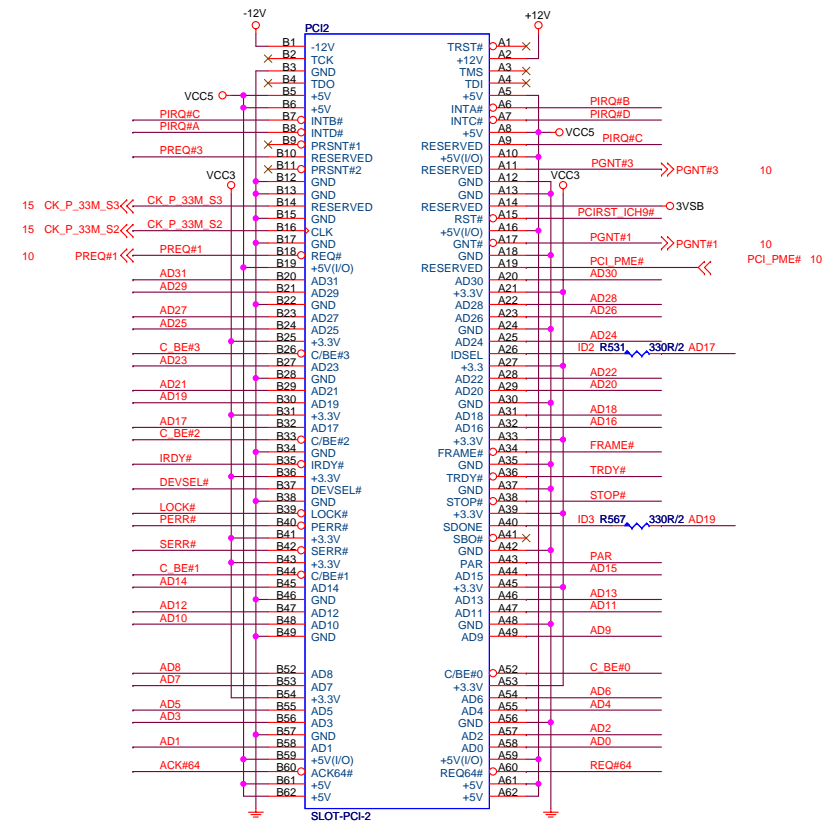
Size Custom	Document Description	Rev 0A
STAC9227		
Date: Thursday, September 27, 2007		

PCI_Express X4 Slot
(Share with PCI_E x1 Slots)



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Size Custom	Document Description PCIE x16, x4, x1 & Bus Switch	Rev 0A
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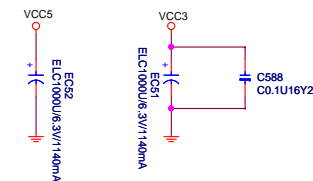
PCI SLOT 2 (PCI VER: 2.2 COMPLY)

IDSEL = AD17

MASTER = PREQ#1

PIRQ#B

PCI SLOT DECOUPLING CAPACITORS

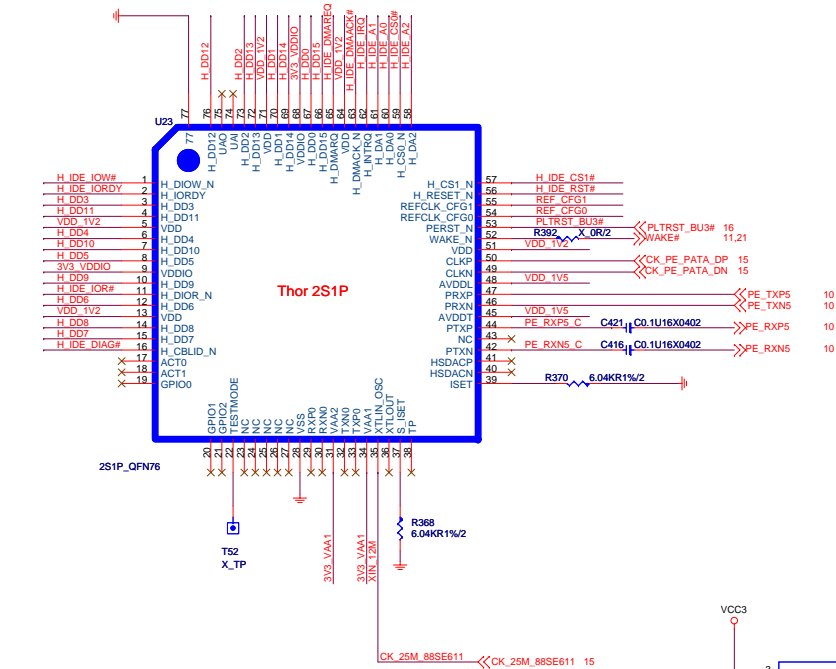


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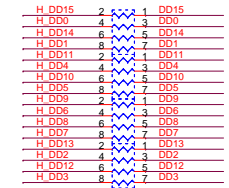
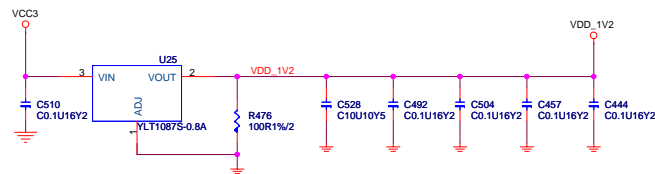
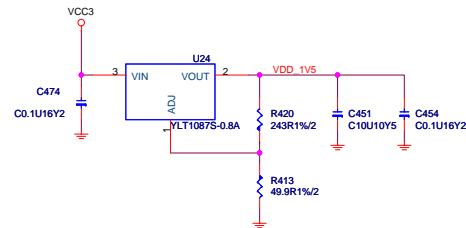
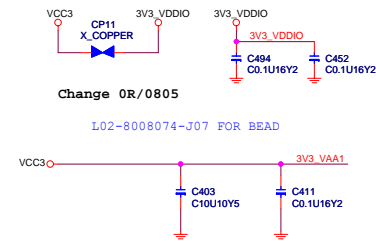
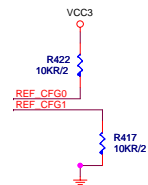
	Document Description
	PCI Slot 1 & 2

Rev
0A

Hi-Speed PCIE to SATA/PATA Bridge



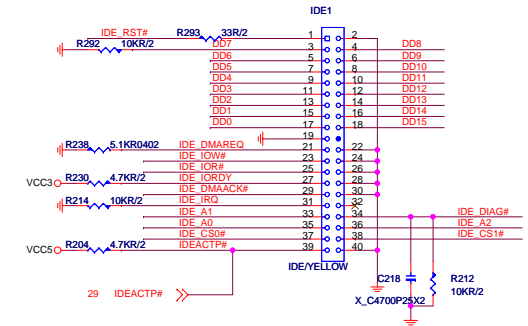
```
REF_CFG[1:0] =  
00:20MHz  
01:25MHz
```



RN43	8P4R-33R/2
RN38	8P4R-33R/2
RN36	8P4R-33R/2
RN41	8P4R-33R/2

H IDE IOW#	R423	22R/2	IDE IOW#
H IDE IOR#	R385	22R/2	IDE IOR#
H IDE A2	R433	22R/2	IDE A2
H IDE A1	R449	22R/2	IDE A1
H IDE A0	R429	22R/2	IDE A0
H IDE DMAACK#	R464	22R/2	IDE DMAACK#
H IDE CS0#	R434	22R/2	IDE CS0#
H IDE CS1#	R414	22R/2	IDE CS1#
H IDE RST#	R450	22R/2	IDE RST#

H IDE DMAREQ	R466	82.5R1%/2	IDE DMAREQ
H IDE IORDY	R416	82.5R1%/2	IDE IORDY
H IDE IRQ	R448	82.5R1%/2	IDE IRQ
H IDE DIAG#	R371	82.5R1%/2	IDE DIAG#



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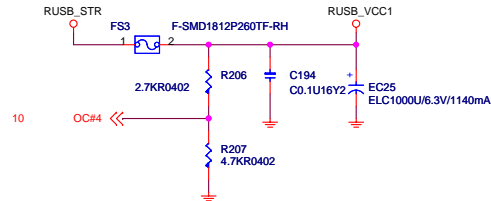
MS-7358

Size Custom	Document Description Marvell 88SE6111 PCIE to PATA/SATA	Rev 0A
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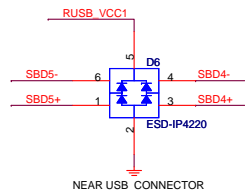
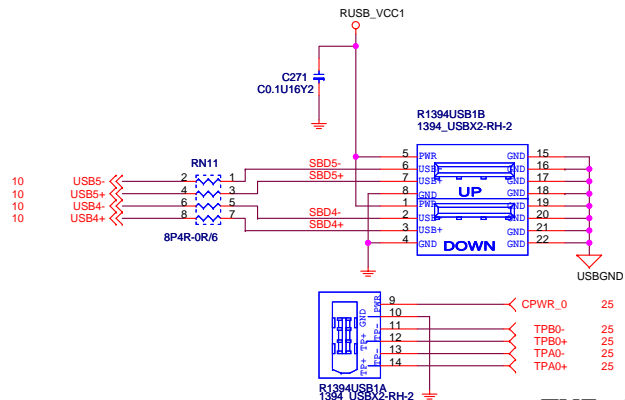
Rear USB Connector

USB POWER FOR PORT 1,2,3,4

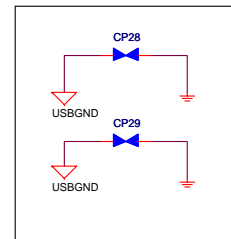
NEAR CONNECTOR



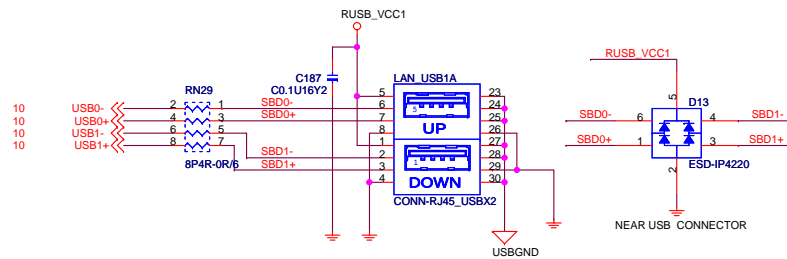
REAR USB PORT 0,1 (1394)



EMI SOLUTION



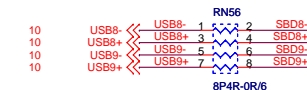
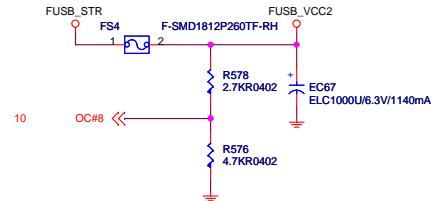
REAR USB PORT 4,5 (With LAN)



Front USB Connector

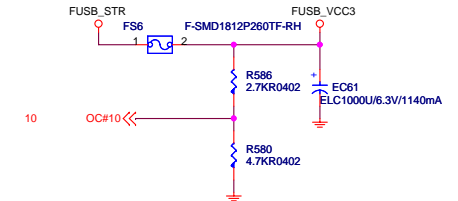
USB POWER FOR PORT 7,8,11,12

NEAR CONNECTOR

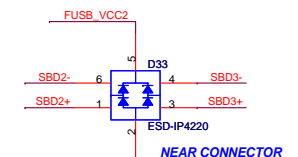
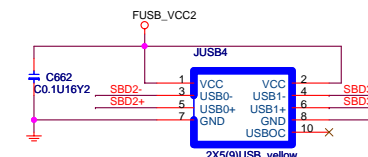


USB POWER FOR PORT 5,6,9,10

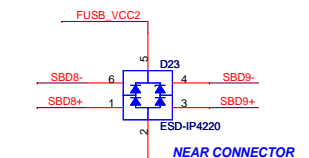
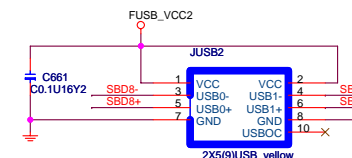
NEAR CONNECTOR



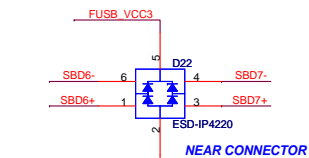
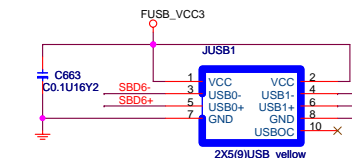
FRONT USB PORT 8,9



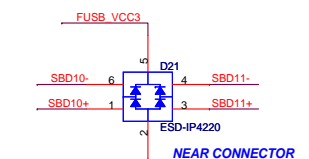
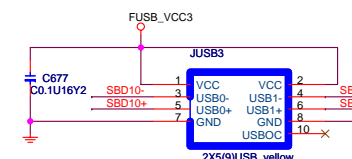
FRONT USB PORT 8,9



FRONT USB PORT 6,7



FRONT USB PORT 10,11

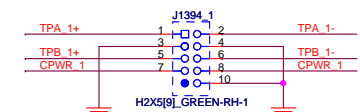
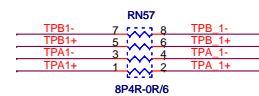
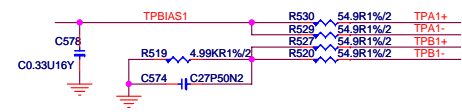
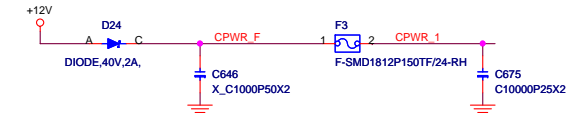
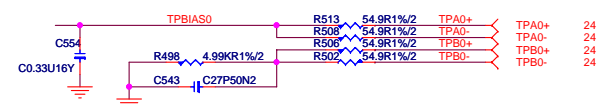
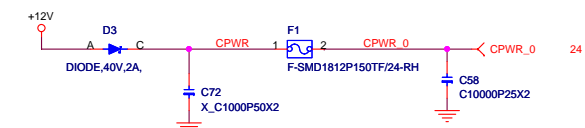
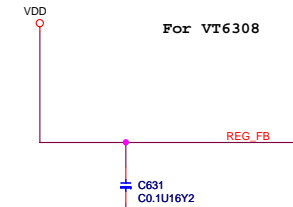
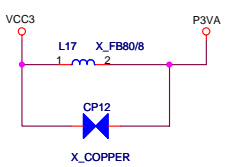
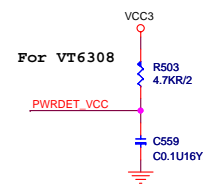
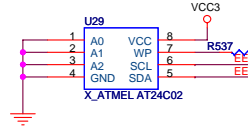
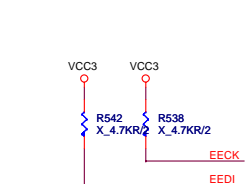
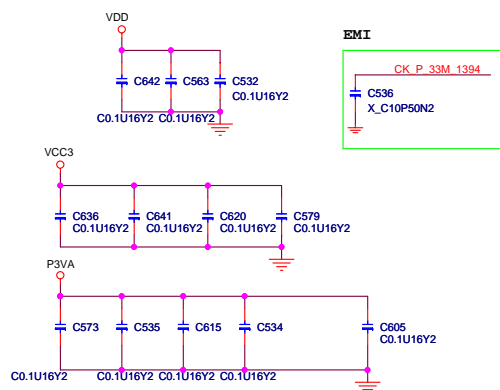
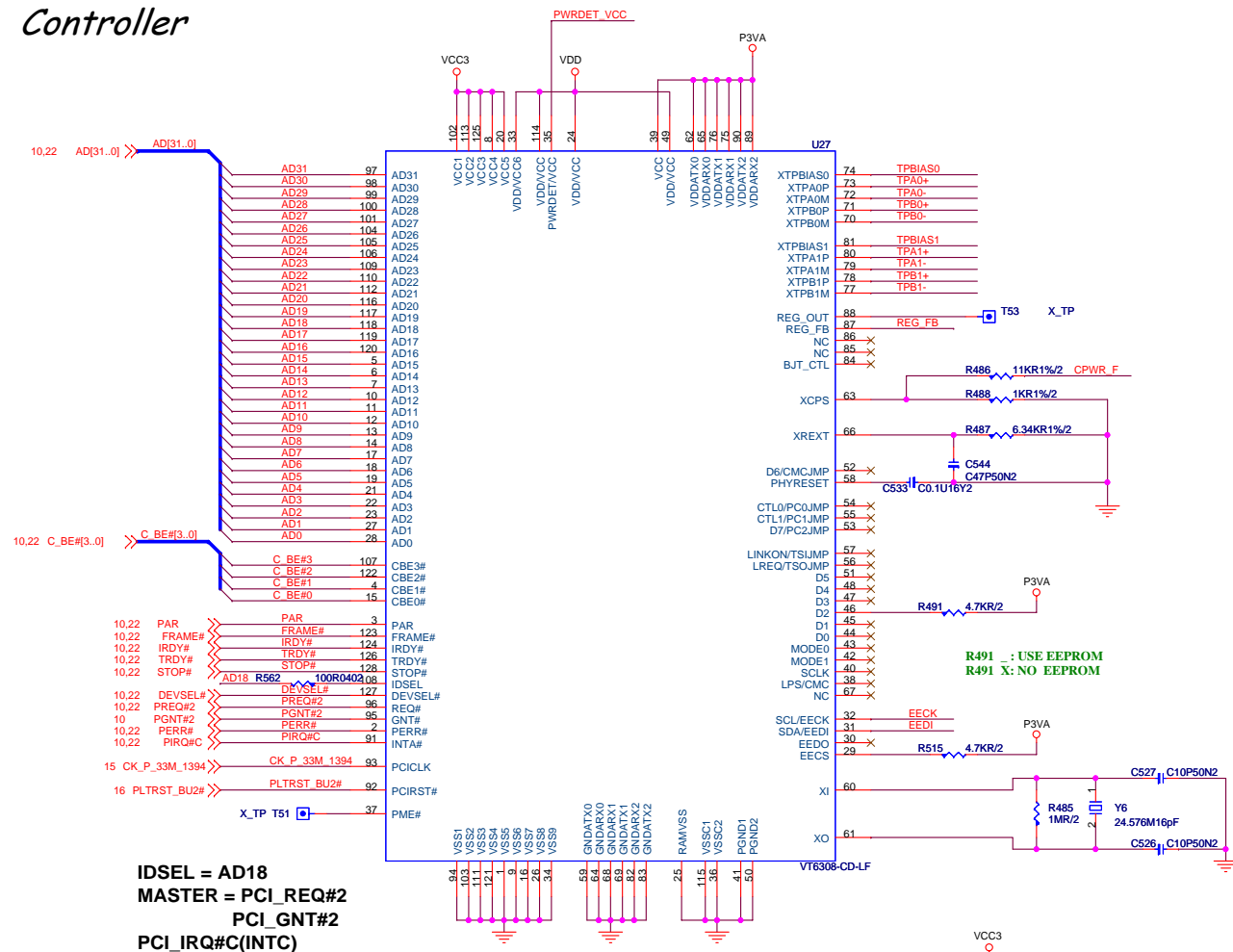


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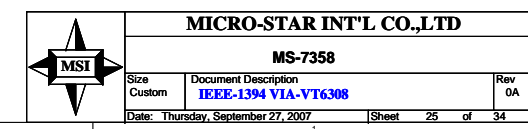
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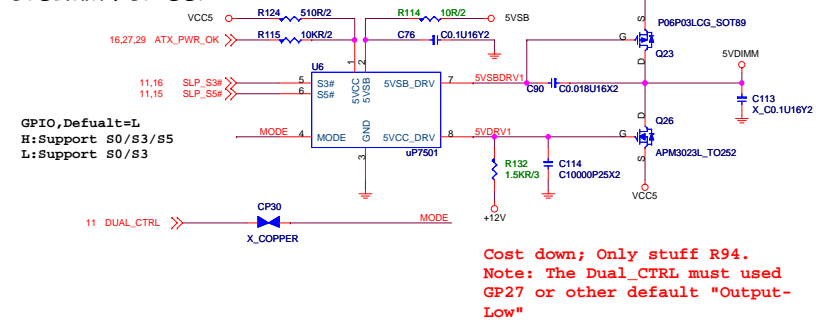
1394a OHCI Link Layer Controller



For Intel 1394 pinheader

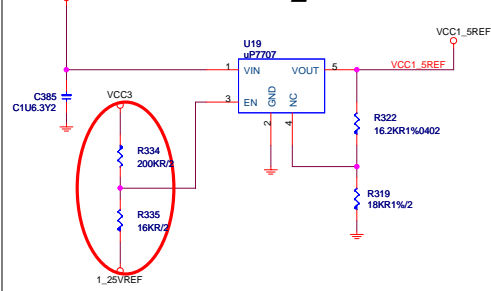


5VDIMM FOR DDR



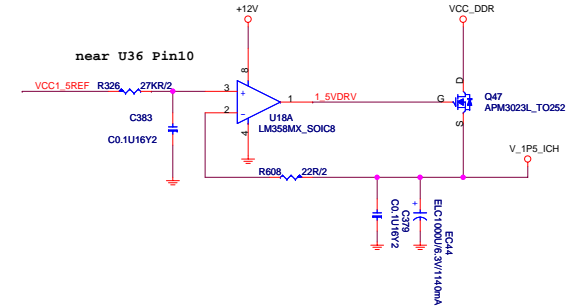
Cost down; Only stuff R94.
Note: The Dual_CTRL must used
GP27 or other default "Output-
Low"

VCC1_5REF

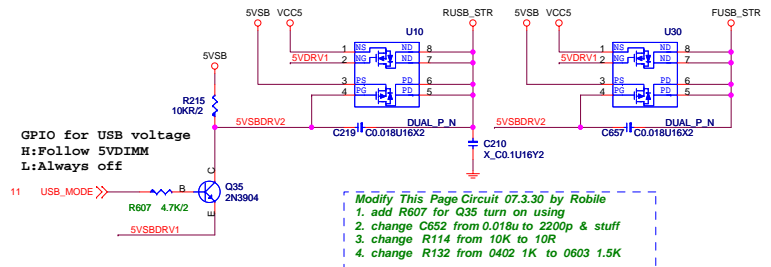


Let 1.25V and 1.5V at the same time
power up or power down

SB 1.5V 2.75A



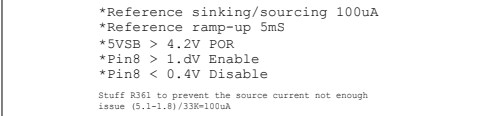
5VSB FOR Rear USB



Modify This Page Circuit 07.3.30 by Robile

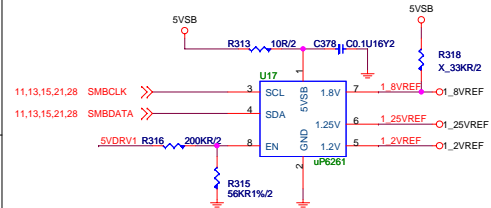
1. add R607 for Q35 turn on using
2. change C652 from 0.018u to 2200p & stuff
3. change R114 from 10K to 10R
4. change R132 from 0402 1K to 0603 1.5K

5VSB FOR Front USB

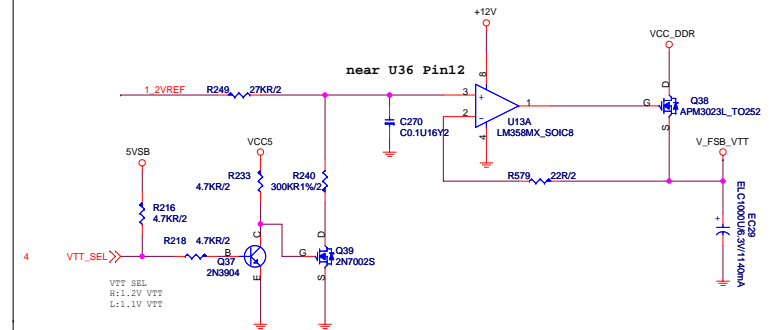


```
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable
```

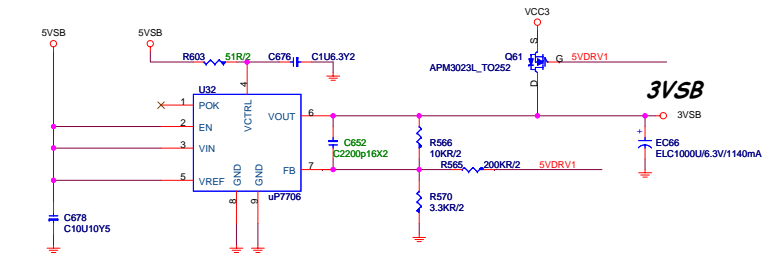
reference Voltage



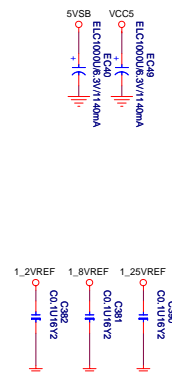
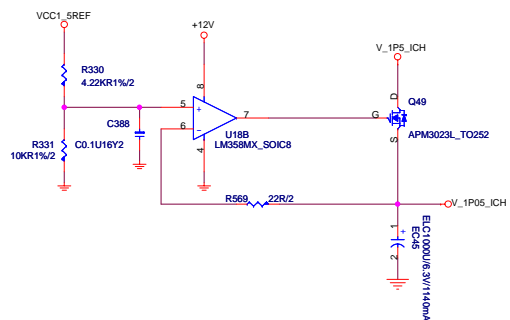
1.2V 5.8A



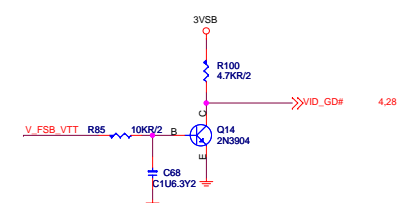
3VSB



SB 1.05V 2A



VID before PWROK >3ms

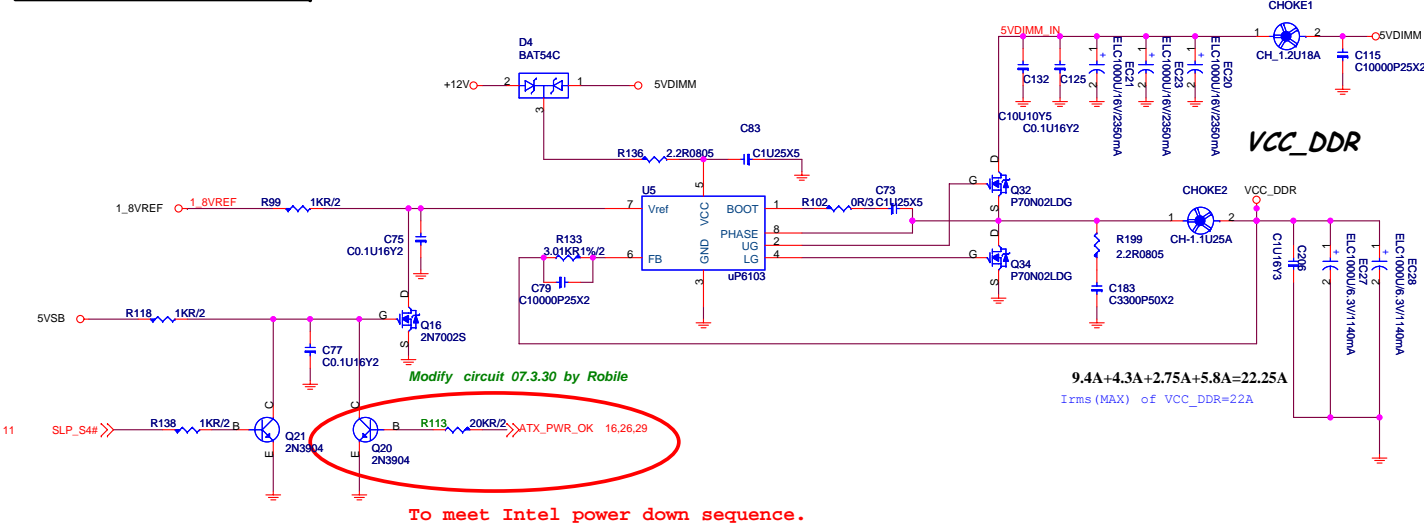


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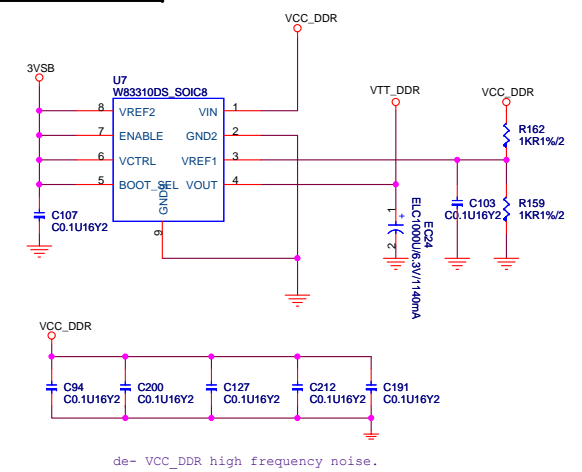
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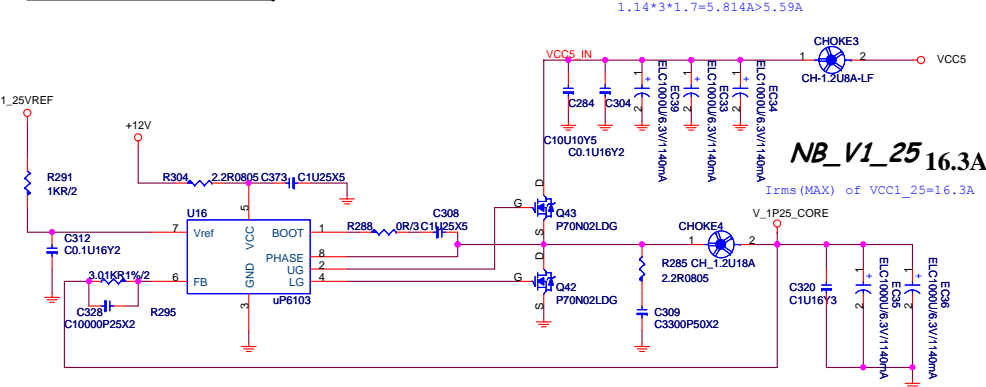
DDR II 1.8V POWER



DDR VTT Power

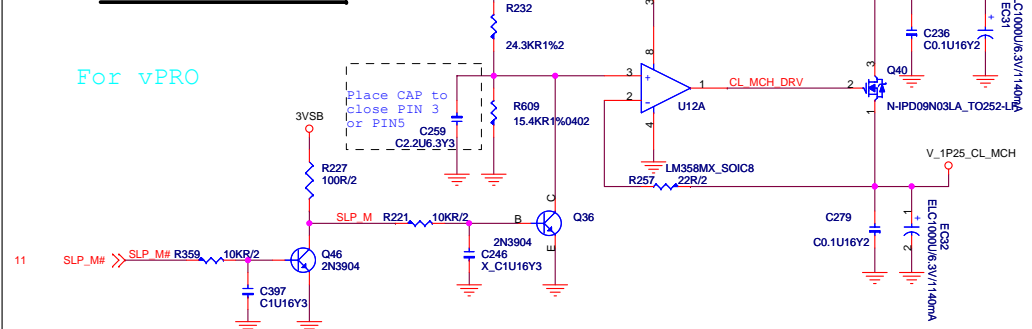


NB 1.25V POWER

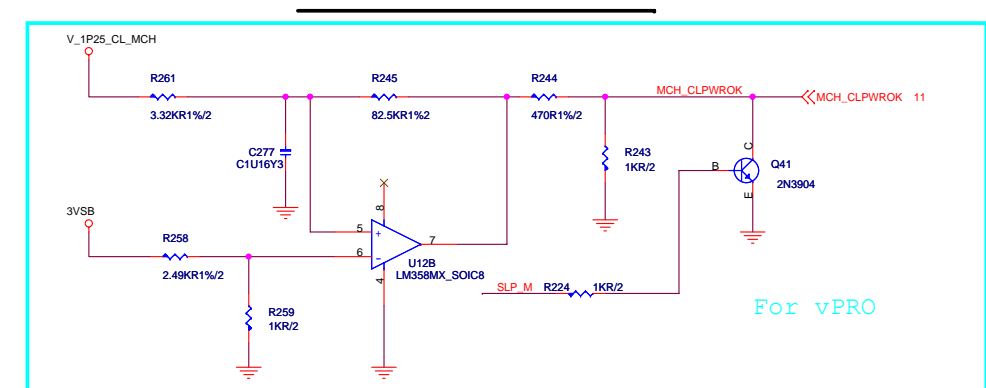


AMT POWER

V_1P25_CL_MCH (4.3A)

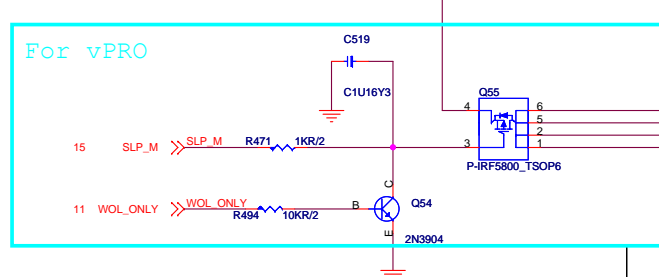


CLINK PWROK GENERATION



V_3P3_CL

(711mA)



For ViiV



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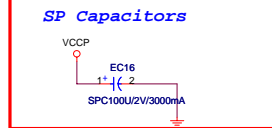
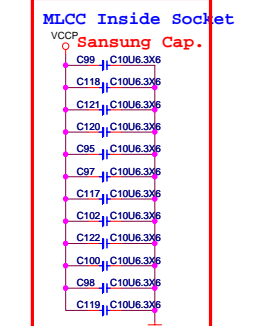
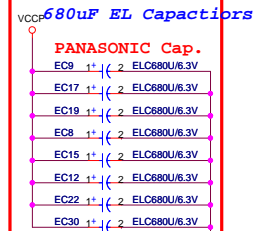
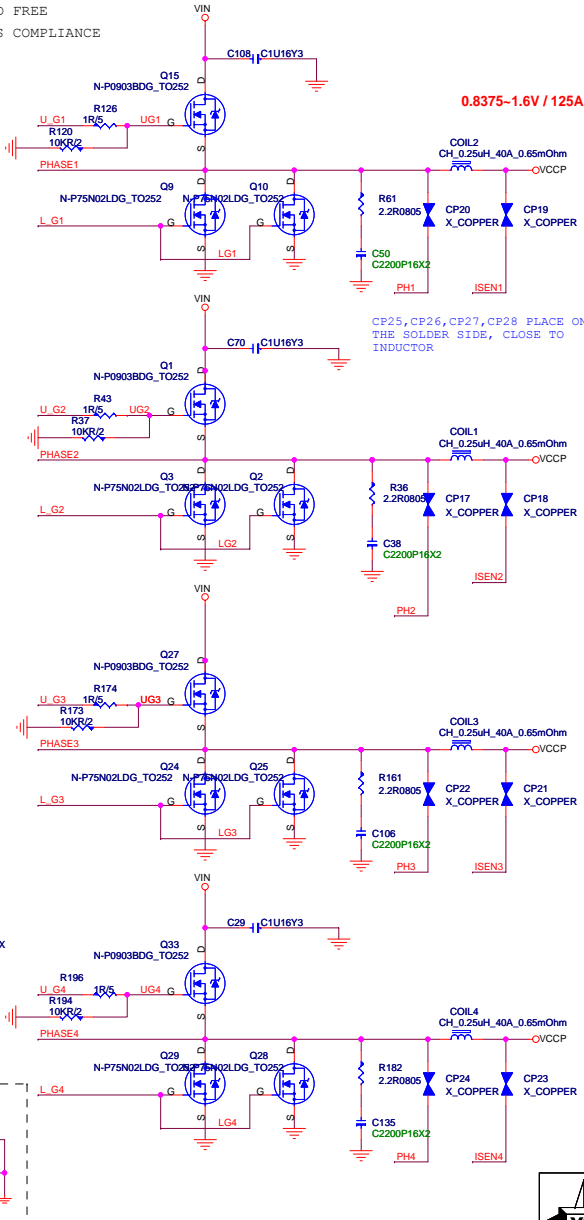
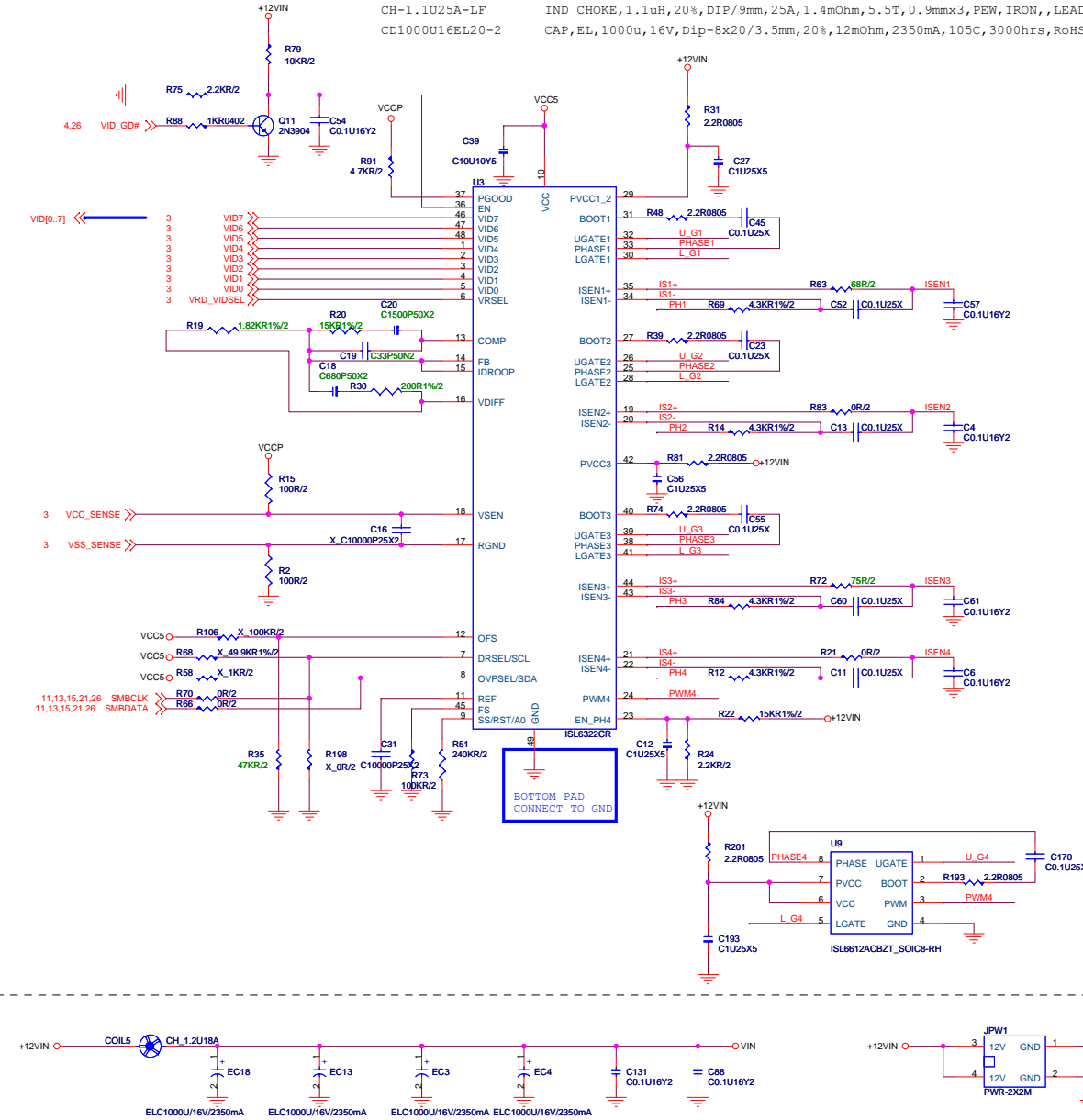
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Voltage Regular Module

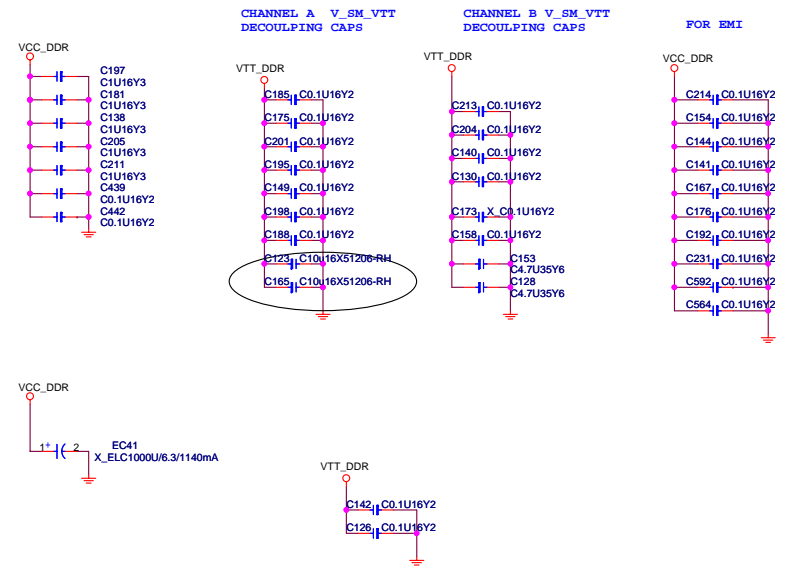
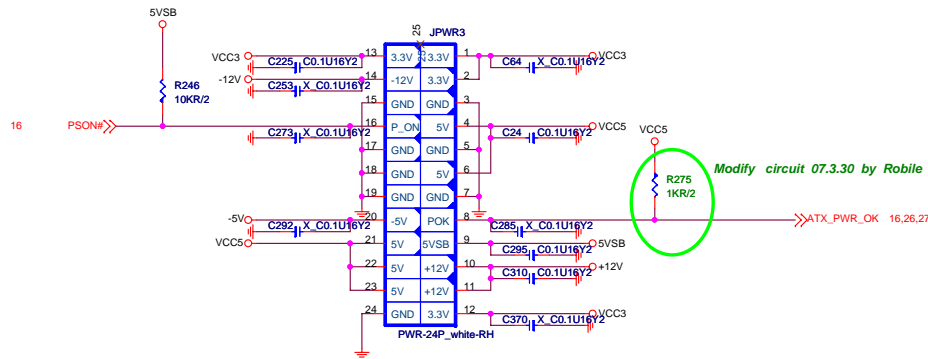
N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V/25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pF, Qg=50nC, Vds=25V, Vgs=±20V, RoHS COMPLIANCE
mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(①10V, 30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pF, Qg=140nC, Vds=25V, Vgs=±20V, RoHS COMPLIANCE
ESR<13mΩ, Ripplecur<6100mA, Lc. <500uA, SPEC series, RoHS compliance
SMD CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, , PEW, FERRITE, SQUARE, RoHS COMPLIANCE
ESR<12mΩ, Ripplecur<2350mA, 105C, longlife change from 2000hrs to 3000hrs ,KZJ
SMD CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, , LEAD FREE
CAP, EL, 1000u, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE

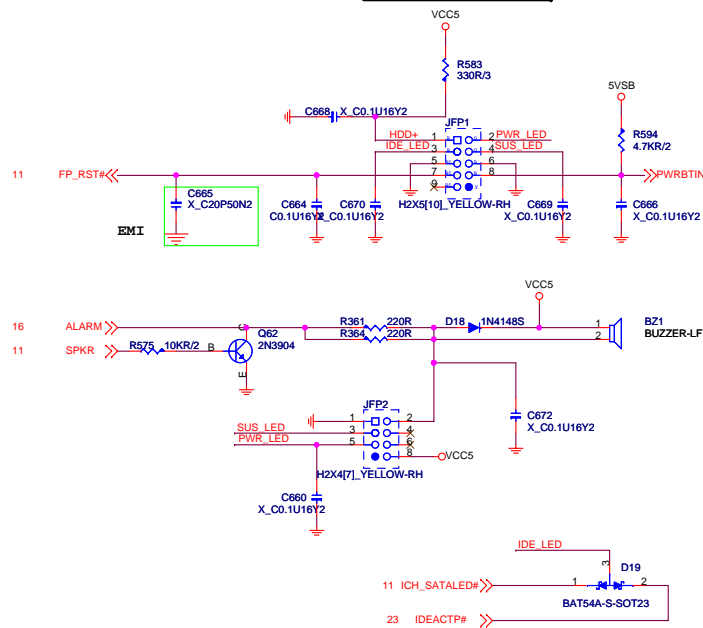


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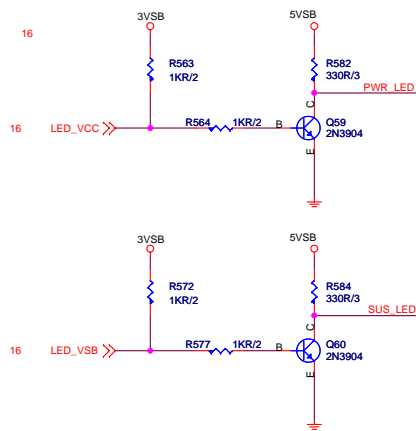
ATX POWER CONNECTOR



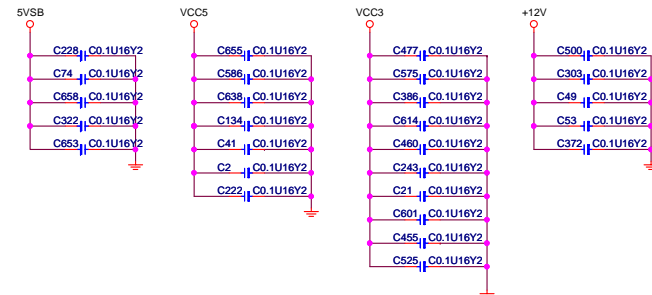
FRONT PANNEL



LED (for Fintek 71882)



Cap. for EMI & Power



MICRO-STAR INT'L CO.,LTD			
MS-7358			
Size	Document Description	Rev	
Custom	ATX PWR-Connector & Front Panel	0A	
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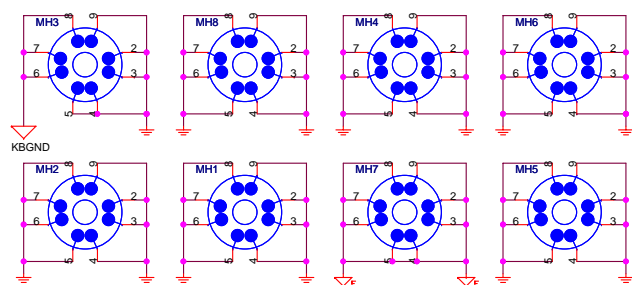
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



Simulation

